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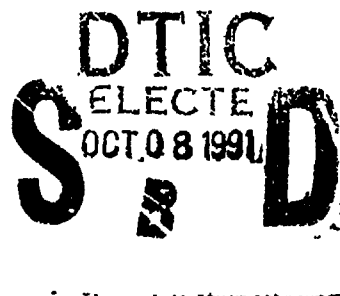
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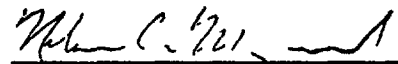
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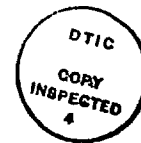
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## FOREWORD

This Final Technical Report, Analytyx Document Number A80808R, is submitted under contract F1962-84-C-0036 corresponding to CDRL item 110/111 of Sub-line Item 0002.



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## **I. INTRODUCTION**

This report provides a technical description of the major items produced under the Space Experiments contract: the CRRES Main electronics packages, the HILAT custom power converters with enclosures (Bert and Ernie), the SSIES-2 Main Electronics Packages (MEP), and the SSIES-2 Ground Support Equipment (GSE). CRRES and HILAT instrument electrical designs (except power supplies), and CRRES software were not done as part of this contract, and are not discussed in this report.

### **I.1 Program Background**

The Space Experiments Program is a collection of many loosely related efforts. Analytyx has been performing design and development work on the DMSP satellite efforts ( SSIES and SSIES-2) since 1980, and has delivered flight hardware and software for three (3) SSIES MEPs, and one (1) SSIES-2 MEP on two other contracts. Two (2) sets of Ground Support Equipment (GSE) were also previously designed and delivered for the SSIES (S8 - S10) flight systems. The equipment delivered under this contract represents an enhanced capability from earlier SSIES systems. The CPU subsystem of the SSIES-2 units has an increased memory complement (PROM - 6k words vs. 4 k words and RAM 16 k words vs. 1.25 k words), and more significantly, has added the option to upload replacement flight software if desired.

The Ground Support Equipment (GSE) developed under this contract provides enhanced operations, including an automated test capability, that allows an SSIES-2 MEP to undergo a complete functional test at the press of a button, the addition of engineering units options to EST and downlink data displays, and the ability to upload software programs to the flight MEP units.

The CRRES Langmuir Probe Main Electronics Box represents a unique cooperative effort, involving Analytyx (AES), AFGL, and the University of California at Berkeley (UCB). Electrical designs for all except the power converters were furnished by the UCB team members, while AFGL provided GSE construction, flight grade microcircuits, and general program coordination. Analytyx was responsible for the mechanical design, power converter design, printed wiring board layouts, and spaceflight quality manufacturing.

The HILAT/Shuttle custom power converters with enclosures were based on the designs used for the SSIES-2 units. The two flight units delivered consisted of 6" x 6" x 6" enclosures, that were split into two distinct

compartments. The base of each unit contained a low power custom power converter, while an open volume (equivalent in size to the stack of boards used in an SSIES-2) was made available for customer circuitry to be added.

## 1.2 Analytyx Reference Documents

### ----- CRRES -----

A80814R      CRRES Langmuir Probe Main Electronics Box  
                 R&D Equipment Information Report  
                 S/N001      October 10,1988

A80815R      CRRES Langmuir Probe Main Electronics Box  
                 R&D Equipment Information Report  
                 S/N002      October 10,1988

### ----- HILAT -----

A80812R      HILAT Bert Electronics Package  
                 R&D Equipment Information Report  
                 S/N001      October 10,1988

A80813R      HILAT Ernie Electronics Package  
                 R&D Equipment Information Report  
                 S/N002      October 10,1988

### ----- SSIES - 2 MEP H/W -----

A70201R      SSIES-2 Plasma Monitor System Main Electronics Package  
                 R&D Equipment Information Report  
                 (All units)      October 10,1988

A70306R      SSIES-2 Plasma Monitor System Main Electronics Package  
                 R&D Equipment Information Report  
                 S/N001      June 23,1986

A70307R      SSIES-2 Plasma Monitor System Main Electronics Package  
                 R&D Equipment Information Report  
                 S/N002      March 16,1987

A70308R      SSIES-2 Plasma Monitor System Main Electronics Package  
R&D Equipment Information Report  
S/N003      May 4,1987

A70309R      SSIES-2 Plasma Monitor System Main Electronics Package  
R&D Equipment Information Report  
S/N004      September 22,1988

A80820R      SSIES-2 MEP Drawing Package  
August 30,1988

----- SSIES - 2 MEP S/W -----

A80409R      SSIES-2 MEP Software Generation Manual  
February 21,1991

A90601R      SSIES-2 Plasma Monitor System Main Electronics Package  
Flight Firmware Documentation  
S/N003      May 4,1987

A50702R      SSIESDAT Downlink Data Interpretation  
July 25,1985

A60603R      SSIES-2 Command Design & Constraints  
June 5,1986

A60605R      Block Loading of the SSIES-2 MEP  
June 6,1986

----- SSIES - 2 GSE H/W & S/W -----

A80811R      SSIES-2 Plasma Monitor System Ground Support Equipment  
R&D Equipment Information Report  
S/N001&2      March 15,1991

A70302R      SSIES-2 Plasma Monitor System Ground Support Equipment  
Software Documentation  
March 5,1987

----- SSIES - 2 MEP Test Procedures -----

A60408R	SSIES-2 Plasma Monitor System Performance Test	April 29, 1986
A60409R	SSIES-2 Plasma Monitor System Functional Test	April 29, 1986
A60410R	SSIES-2 Plasma Monitor System Critical Parameter Monitoring	April 29, 1986
A60411R	SSIES-2 Plasma Monitor System Abbreviated Functional Test	April 29, 1986

----- Miscellaneous Test Reports -----

TR 4417	Report of Electromagnetic Compatibility Test on an SSIES-2 Plasma Monitor System Main Electronics Package (Sanders Associates)	May 23,1986
21999-87C	Report of Test for Vibration and Shock Testing of CRRES Experiments AFGL 701-13, 14 and DMSP SSIES-2 ( National Technical Systems)	May 28,1986
22776-87M	Report of Test for Vibration Testing of SSIES-2 Satellite Equipment Series	October 24,1986

## **2. CRRES LANGMUIR PROBE MAIN ELECTRONIC BOX**

### **2.1 Introduction**

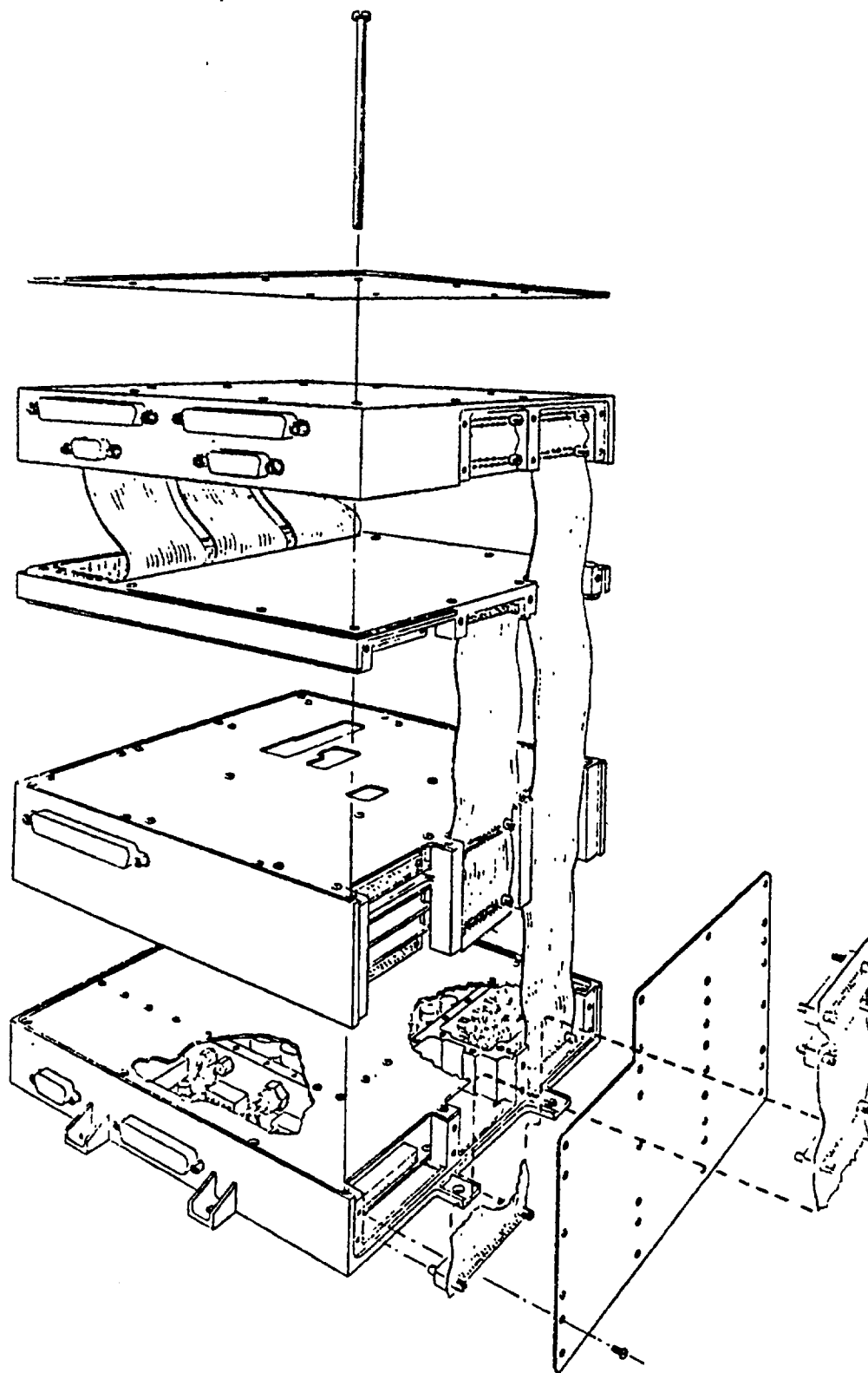
This section describes the design developed for the Combined Release and Radiation Effects Satellite (CRRES) Langmuir Probe Main Electronics Box (AFGL Experiment 701-14A) package, S/Ns 001 and 002. The CRRES unit constitutes line item 0001AC-1 under this contract. Both the general mechanical design of the package and the detailed electrical design of the power converter subsystem are described.

### **2.2 Mechanical Description**

The CRRES Langmuir Probe Main Electronics is enclosed in a 9.5" x 9.5" x 5", 451 cubic inch aluminum housing (refer to figure 2-1 for an exploded view). These dimensions exclude mounting pads, external connectors, and hardware protrusions. The assembled unit weighs 16.2 pounds. The unit is constructed of 6061-T6 aluminum, held together and fastened to the mounting surface by stainless steel screws and bolts.

The structure is an assembly of four separate sections each 9.5" x 9.5". The four sections are each milled from a single piece of aluminum that interlock and stack on top of one another and are bolted together with twelve #8-32 bolts. Eight pads are provided on the bottom structure (the power supply housing) at the mounting surface with .217-.225 diameter mounting holes enabling the unit to be fastened to the spacecraft with #10-32 or M5 hardware.

The mounting surface is finished with electrically conductive chemical film per MIL-C-5541 class 3. The remainder of the surfaces (top and four sides) are finished with Chemglaze Z306, a flat black acceptably-low outgassing polyurethane paint made by Hughson Chemical. External interconnect has been provided by rectangular type "D" style gold plated non-magnetic brass shell connectors that which meet the applicable sections of MIL-C-85049/MIL-C-24308.



**Figure 2-1 CRRES Mechanical Housing Exploded**

The CRRES unit Main Electronics and Power Converter electronics are partitioned onto twelve multilayer, two sided, .062 thick Printed Wiring Board (PWB) assemblies. The PWBA's are packaged into four separate sub-assemblies; the Power Supply assembly #E2271, the Digital I/O Frame assembly #E2253, the I/O Frame assembly #E2298 and the Analog Frame assembly #E2246. The mechanical packaging scheme provides shielding between compartments.

Interconnect and power distribution between compatible PWBA's is accomplished through 70 position Airborn pc board & flex circuit connectors with isolated flex circuit backplanes. Interconnect between incompatible PWBA's is accomplished by using flex circuit backplanes (and 70 position Airborn connectors) attached to wall mounted feedthrough filter capacitors between the shielded incompatible sections.

The Power Supply assembly (the bottom assembly) is packaged in a housing with three separate compartments. An "L" shaped compartment houses the power converters relay section. Spacecraft power is supplied to this section from an external connector and fed onto the relay circuitry. A filter wall separates the relay and the main compartment housing the Buckswitcher circuitry. Power from the main compartment is fed through a filter wall to the isolated analog backplane compartment and back to the relay section for distribution to the digital backplanes.

The Digital I/O Frame assembly is packaged in an "I-beam" style frame. The Burst Processor PWBA is mounted to the bottom side of the frame with a full shield plate between it and the power converter. Mounted in a stack on the top side of the frame is the Burst Processor PWBA and two Memory PWBA's. Flex circuit backplanes are used on the opposite side from the power input to interconnect the digital PWBA's.

The I/O Frame assembly has an upside down tray type frame with the I/O PWBA mounted in the tray facing the Digital Frame assembly with a shield between them. The frame forms a full shield for the electronics above and all interconnect between the upper analog and lower digital electronics is routed through a filter wall located in the I/O frame. Flex circuits cabling is used between the filter walls and the PWBA'S.

The Analog Frame assembly is packaged in an "I-beam" style frame with one PWBA mounted to each side of the frames center wall. Mounted to the bottom side is the Filter PWBA and the top houses the Analog PWBA.

A cover is fastened to the top of the Analog Frame assembly, access covers are fastened over the backplane compartments and as described above the four sections are bolted together with #8-32 bolts through the upper three frames and into the Power Converter assembly.

## **2.3 CRRES Power Converter**

### **2.3.1 Introduction**

Figure 2-2 shows a block diagram of AFGL 701-14A power converter. The selected topology is a single-ended buck regulator driving a push-pull converter with regulation derived from duty-cycle variation of the fixed frequency 50 kHz quasi square wave. Given constraints of size, weight, efficiency, and regulation, the highest possible frequency was used. This reduces the size of the magnetic and capacitive components and eases the filtering burden. Selecting a higher frequency of operation would not be advisable due to the large number of outputs and the absence of secondary regulation, because the higher frequency reduces the transformer turns/volt, reducing the output voltage resolution.

Push-pull operation ensures a reasonably low output impedance over single-ended designs for better output regulation. Regulation is better than +4% for line, half to full load and temperature variation, except for the +5V output, which is less than +0.5% and the -5.2V output which is less than +2%.

All positive and respective negative voltages share common returns but are isolated from all other returns within the converter. Current monitors utilize current transformers for sensing and have isolated returns within the converter.

Power Transformers utilize electrostatic shields between the primary and secondaries for enhanced common mode noise rejection on the +35V and two +12V floating outputs.

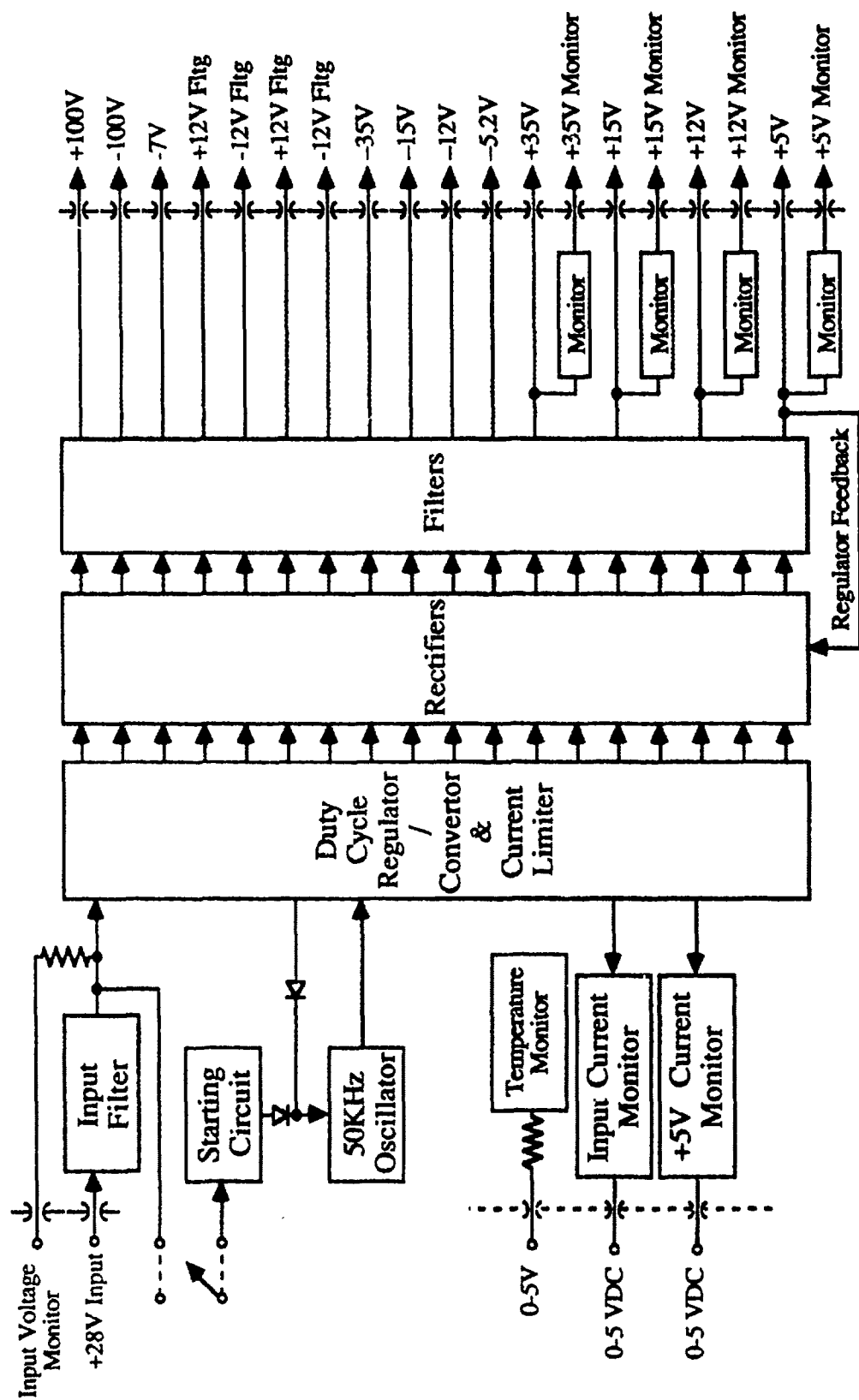


Figure 2-2 CRRES Power Converter Block Diagram

### **2.3.2 Input Section.**

A diode in series with the input prevents damage against polarity reversal. An inrush current limiter circuit at the input of each converter serves two purposes:

1. Protects against positive high voltage input transients.
2. Since the diode across the input exhibits .6V drop in its reverse direction it protects the input relay from high voltage buildup of the input chokes when the relay opens and the choke fields collapse.

### **2.3.3 Overload Protection.**

Two modes of protection are utilized:

1. The +35V, & two 12V floating outputs are protected individually by separated fold-back limiters on each output. Overloading or shorting of these outputs will have no effect on any other output.
2. All of the other outputs are protected from overload or short circuit by current sensing the primary current with a current transformer. The secondary of the current transformer produces a voltage proportional to primary current which, on overload, overrides the pulse width regulator reducing the pulse width in proportion to the degree of overload. Under these conditions all outputs will drop proportionately.

### **2.3.4 Output Converter**

The output converter is driven by the square wave oscillator and produces the near perfect square waves essential for low output impedance, hence, good output regulation. Load regulation is then entirely dependent on the dynamic impedance of the rectifier diodes except for the +5V output which is held constant by the regulator.

### **2.3.5 Backup Converter.**

The backup supply is somewhat similar to the main converter in that it has an in-rush limiter, input filter, regulator, and power converter. The

main differences are that a linear regulator is used in conjunction with a fold-back current limiter and the converter consists of a self-driven oscillator which produces the isolated + 15V outputs. The output is then diode gated to the +15V output rectifiers on the main converter.

### **3. HILAT BERT ELECTRONICS PACKAGE**

#### **3.1 Introduction**

This section describes the electrical power converter design approach for the AFGL HILAT Bert experiment package. This unit constitutes half of sub-line item 0001AB under this contract, and is defined by Analytyx part number 59700-2340-2.

#### **3.2 Power Converters**

A block diagram for the Bert converter is shown in Figure 3-1. This converter and the Ernie converter described in Section 4 are similar in design. Both converters have floating outputs.

##### **3.2.1 Input Section**

The input filter serves the following functions:

- o Reduction of inrush current required to charge the input capacitors
- o Filters input ripple above 1 KHz
- o Prevents the 30 KHz switching frequency ripple from feeding back onto the spacecraft power bus.

The selected regulator topology is a switching regulator with regulation derived from duty cycle variation of the fixed frequency 30 KHz quasi-squarewave. The resulting filtered and regulated DC voltage is then chopped and transformer coupled to the outputs. Current monitors utilize high-efficiency current transformers for current sensing and have isolated returns within the converter

Input regulation, designed to regulate out input variations such as the 24 V to 32 Vdc plus the superimposed input audio imposed by CS01, CS02 is achieved by high efficiency switching regulation. Regulation is achieved by varying the duty cycle of a switching transistor in series with the input line.

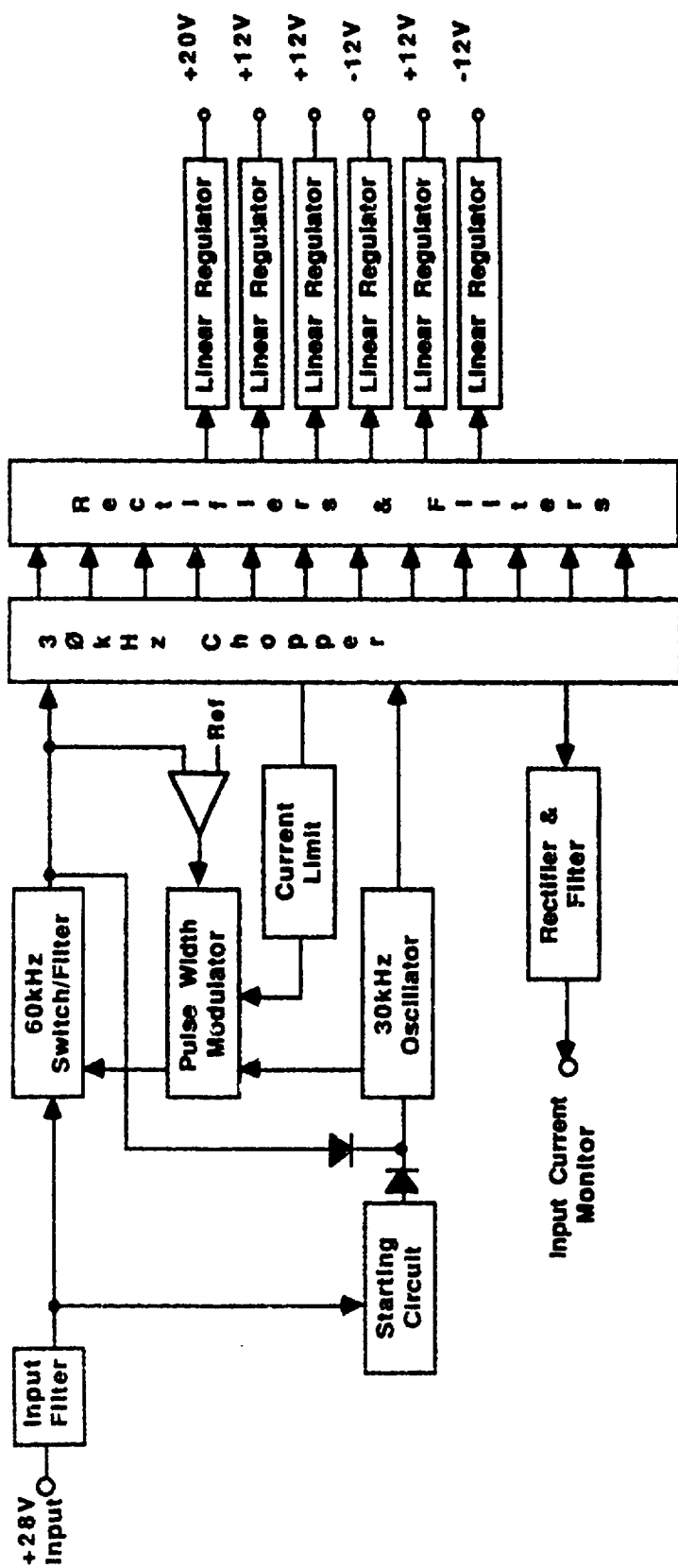


Figure 3-1 Bert Power Converter Block Diagram

The pulse width or on time of the pass element is varied in accordance with the regulation requirements. The ac waveform is then averaged and converted to DC with a filter, consisting of a choke, a capacitor and a recycle diode. Referring to Figure 2.5-3, a ramp is generated by an integrator derived from the oscillator and superimposed on the comparator. Duty cycle variation is achieved by comparing a point on the slope of the ramp with a voltage derived from the error amplifier. The error amplifier in turn compares the output voltage with a reference, adjusting the on time of the duty cycle switch until a point of equilibrium is achieved.

Current limiting is achieved when the voltage from the current transformer exceeds the reference voltage, overriding the amplifier output, reducing the on time of the switch, reducing the input current until a point of equilibrium is reached for that particular overload condition.

### 3.2.2 Output Section

All positive and negative voltages share common returns but are be isolated from all other returns within the converter. Sensitive circuits in the system are provided with secondary linear regulation.

This stage actually performs the DC to AC conversion of the input and also provide input-output isolation. The various outputs are then converted to the proper voltages, rectified, filtered and passed on to the regulators. Operating in the square wavemode with the transformer in its linear rather than saturated mode for lower peak currents results in reasonably good efficiency, usually about 80-85%, the losses being mostly due to transistor saturation drop with some additional loss due to transistor switching time.

### 3.2.3 Overload Protection.

Two modes of protection are utilized:

1. All outputs are protected individually by separated fold-back limiters on each output. Overloading or shorting of these outputs has no effect on any other output.
2. A primary current limiter is used to prevent damage to the input section of the converter or excessive spacecraft power bus loading if multiple outputs are shorted.

### **3.2.4 Performance Summary.**

The design has achieved a total system efficiency on the order of 53% even at the low power level with eight outputs. The converter has a very high bandwidth and a very high ripple rejection rate that meets all MIL Standards for conducted emissions and audio susceptibility. For high reliability a minimum parts count was also achieved.

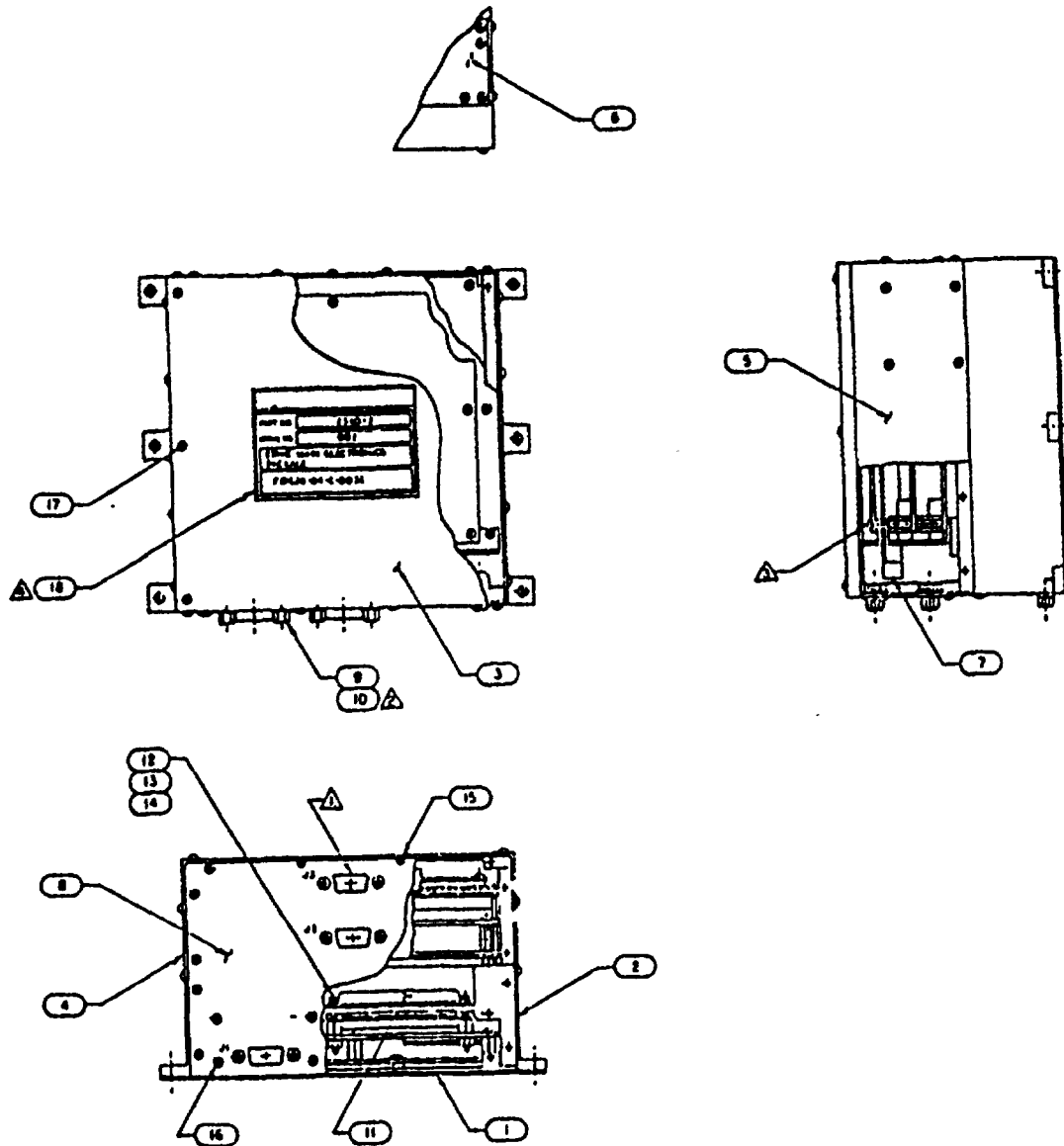
### **3.3 Mechanical Description**

BERT is enclosed in a 6" x 6" x 4", 144 cubic inch aluminum housing (shown in figure 3-2). These dimensions exclude mounting feet, external connectors and hardware protrusions. The unit weighs about 4 1/2 lbs. The structural elements of the unit are of 6061-T6 aluminum, held together with stainless steel hardware. The mounting surface and all interior surfaces are finished with electrically conductive chemical film per MIL-C-5541, class 3. The remainder of the exterior surfaces are finished with Chemglaze Z306, a flat black acceptably-low outgassing polyurethane paint made by Hughson Chemical. External interconnect has been provided by rectangular type "D" style gold plated non-magnetic brass shell connectors which meet the applicable sections of MIL-C-85049/MIL-C- 24308.

The mechanical structure is an assembly of plates and covers fastened to a single piece machined housing. The assembly forms two separate sections, the power converter and the main electronics sections. The power converter is a separable assembly mounted to the base plate located at the bottom of the structure for maximum heat transfer. When the assembled power converter is plugged into the bottom of the main housing it is mated to a bulkhead mounted 50 pin connector that distributes the power to the electronics stack section in the upper part of the structure.

The electronics stack section has been designed to house three customer supplied electronics boards. A shield plate is provided with the unit for customer installation within the upper stack.

**Figure 3-2 Bert Mechanical Assembly Diagram**



## **4. HILAT ERNIE ELECTRONICS PACKAGE**

### **4.1 Introduction**

This section describes the electrical power converter design approach for the AFGL HILAT Ernie experiment package. This unit constitutes half of sub-line item 0001AB under this contract, and is defined by Analytex part number 59700-2340-1.

### **4.2 Power Converters**

A block diagram for the Ernie converter is shown in Figure 4-1. This converter design and the Bert converter described in Section 3 are similar. Both converters have floating outputs.

#### **4.2.1 Input Section**

The input filter serves the following functions:

- o Reduction of inrush current required to charge the input capacitors
- o Filters input ripple above 1 KHz
- o Prevents the 30 KHz switching frequency ripple from feeding back onto the spacecraft power bus.

The selected regulator topology is a switching regulator with regulation derived from duty cycle variation of the fixed frequency 30 KHz quasi-square-wave. The resulting filtered and regulated DC voltage is then chopped and transformer coupled to the outputs. Current monitors utilize high-efficiency current transformers for current sensing and have isolated returns within the converter

Input regulation, designed to regulate out input variations such as the 24 V to 32 Vdc plus the superimposed input audio imposed by CS01, CS02 is achieved by high efficiency switching regulation. Regulation is achieved by varying the duty cycle of a switching transistor in series with the input line. The pulse width or on time of the pass element is varied in accordance with

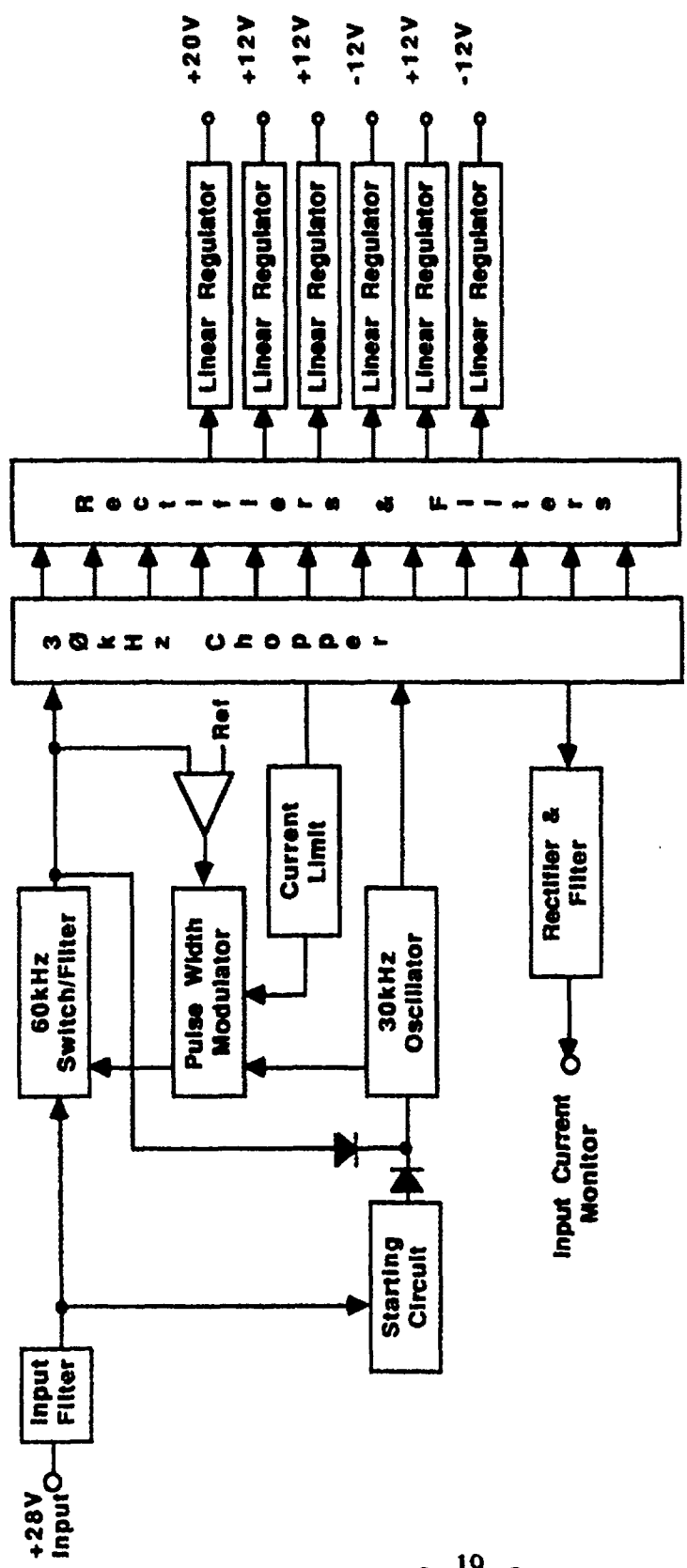


Figure 4-1 Ernie Power Converter Block Diagram

the regulation requirements. The AC waveform is then averaged and converted to DC with a filter, consisting of a choke, a capacitor and a recycle diode. Referring to Figure 2.5-3, a ramp is generated by an integrator derived from the oscillator and superimposed on the comparator. Duty cycle variation is achieved by comparing a point on the slope of the ramp with a voltage derived from the error amplifier. The error amplifier in turn compares the output voltage with a reference, adjusting the on time of the duty cycle switch until a point of equilibrium is achieved.

Current limiting is achieved when the voltage from the current transformer exceeds the reference voltage, overriding the amplifier output, reducing the on time of the switch, reducing the input current until a point of equilibrium is reached for that particular overload condition.

#### 4.2.2 Output Section

All positive and negative voltages share common returns but are isolated from all other returns within the converter. Sensitive circuits in the system are provided with secondary linear regulation.

This stage actually performs the DC to AC conversion of the input and also provides input-output isolation. The various outputs are then converted to the proper voltages, rectified, filtered and passed on to the regulators. Operating in the square wavemode with the transformer in its linear rather than saturated mode for lower peak currents results in reasonably good efficiency, usually about 80-85%, the losses being mostly due to transistor saturation drop with some additional loss due to transistor switching time.

#### 4.2.3 Overload Protection.

Two modes of protection are utilized:

1. All outputs are protected individually by separated fold-back limiters on each output. Overloading or shorting of these outputs has no effect on any other output.
2. A primary current limiter is used to prevent damage to the input section of the converter or excessive spacecraft power bus loading if multiple outputs are shorted.

#### **4.2.4 Performance Summary.**

The design has achieved a total system efficiency on the order of 53% even at the low power level with eight outputs. The converter has a very high band width and a very high ripple rejection rate that meets all MIL Standards for conducted emissions and audio susceptibility. For high reliability a minimum parts count was also achieved.

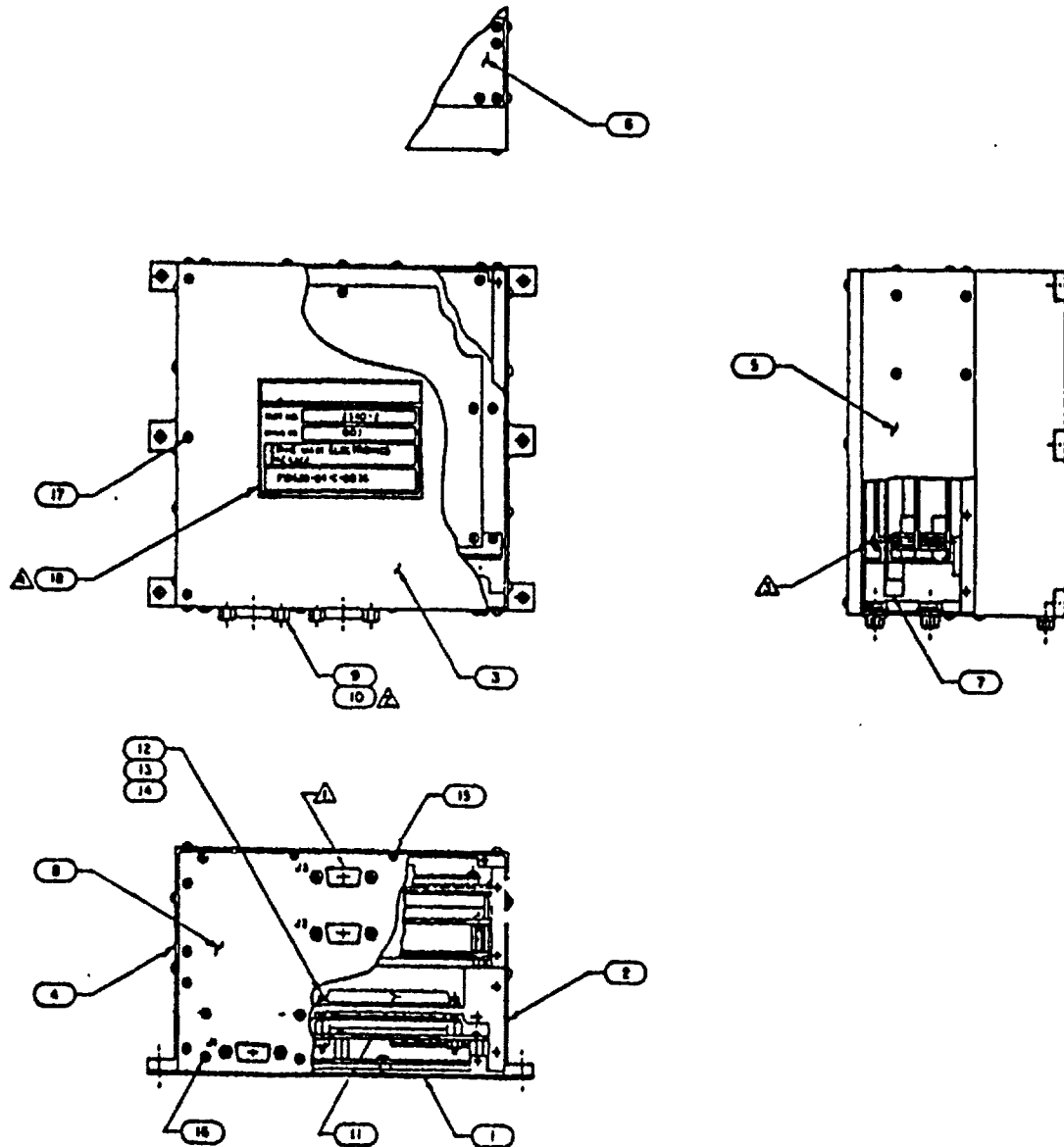
#### **4.3 Mechanical Description**

ERNIE is enclosed in a 6" x 6" x 4", 144 cubic inch aluminum housing (shown in figure 4-2). These dimensions exclude mounting feet, external connectors and hardware protrusions. The unit weighs about 4 1/2 lbs. The structural elements of the unit are of 6061-T6 aluminum, held together with stainless steel hardware. The mounting surface and all interior surfaces are finished with electrically conductive chemical film per MIL-C-5541, class 3. The remainder of the exterior surfaces are finished with Chemglaze Z306, a flat black acceptably-low outgassing polyurethane paint made by Hughson Chemical. External interconnect has been provided by rectangular type "D" style gold plated non-magnetic brass shell connectors which meet the applicable sections of MIL-C-85049/MIL-C- 24308.

The mechanical structure is an assembly of plates and covers fastened to a single piece machined housing. The assembly forms two separate sections, the power converter and the main electronics sections. The power converter is a separable assembly mounted to the base plate located at the bottom of the structure for maximum heat transfer. When the assembled power converter is plugged into the bottom of the main housing it is mated to a bulkhead mounted 50 pin connector that distributes the power to the electronics stack section in the upper part of the structure.

The electronics stack section has been designed to house three customer supplied electronics boards. A shield plate is provided with the unit for customer installation within the upper stack.

**Figure 4-2 Ernie Mechanical Assembly Diagram**



## **5. SSIES-2 PLASMA MONITOR SYSTEM MEP**

### **5.1 Introduction**

This section describes the characteristics of the SSIES-2 Plasma Monitor System Main Electronics Package (MEP). A full system consists of the MEP, a Drift Scintillation Meter (DSM), and associated sensors. The sensors include a spherical electron sensor and three planar-mount ion sensors. The MEP provides microcomputer control of the sensor biases, data sampling, plasma calculations, and spacecraft command and data interfaces.

The information contained herein is relevant to the Prototype, and S/N 001, 002, 003, and 004 Main Electronic Packages delivered for DMSP spacecraft S11, S12, S13, and S14. The Analytix part number for this unit is 59700-2500.

### **5.2 Unit Design Approach**

The function of the Main Electronics Package (MEP) within the SSIES-2 Plasma Monitor system is depicted in figure 5-1. As shown, the MEP contains the single DC-DC converter that supports both internal MEP circuitry and the Drift Scintillation Monitor (DSM). The package provides sweep generator outputs, bias voltages and logarithmic amplifiers for the electron sensor and one of the three ion sensors, the RPA. In addition, the MEP programmable bias supplies support both MEP and DSM requirements.

The MEP processing and control circuitry performs all timing signal generation, data conversion, and formatting for both the MEP and DSM. Finally, the MEP provides all telemetry and command interfacing to the spacecraft.

The MEP block diagram is shown in figure 5-2. The block diagram illustrates the twelve printed wiring boards that are enclosed within the MEP mechanical housing. The boards by location are:

- o Electrometer Interface (A1)
- o Analog/DSM Interface (A2)
- o Sweep Generator (A3)
- o Sweep Control and Bias (A4)
- o OLS Interface (A5)

- o CPU Interface (A6)
- o RAM (A7)
- o CPU (A8)
- o Power Converter Subassembly (A9-A12)

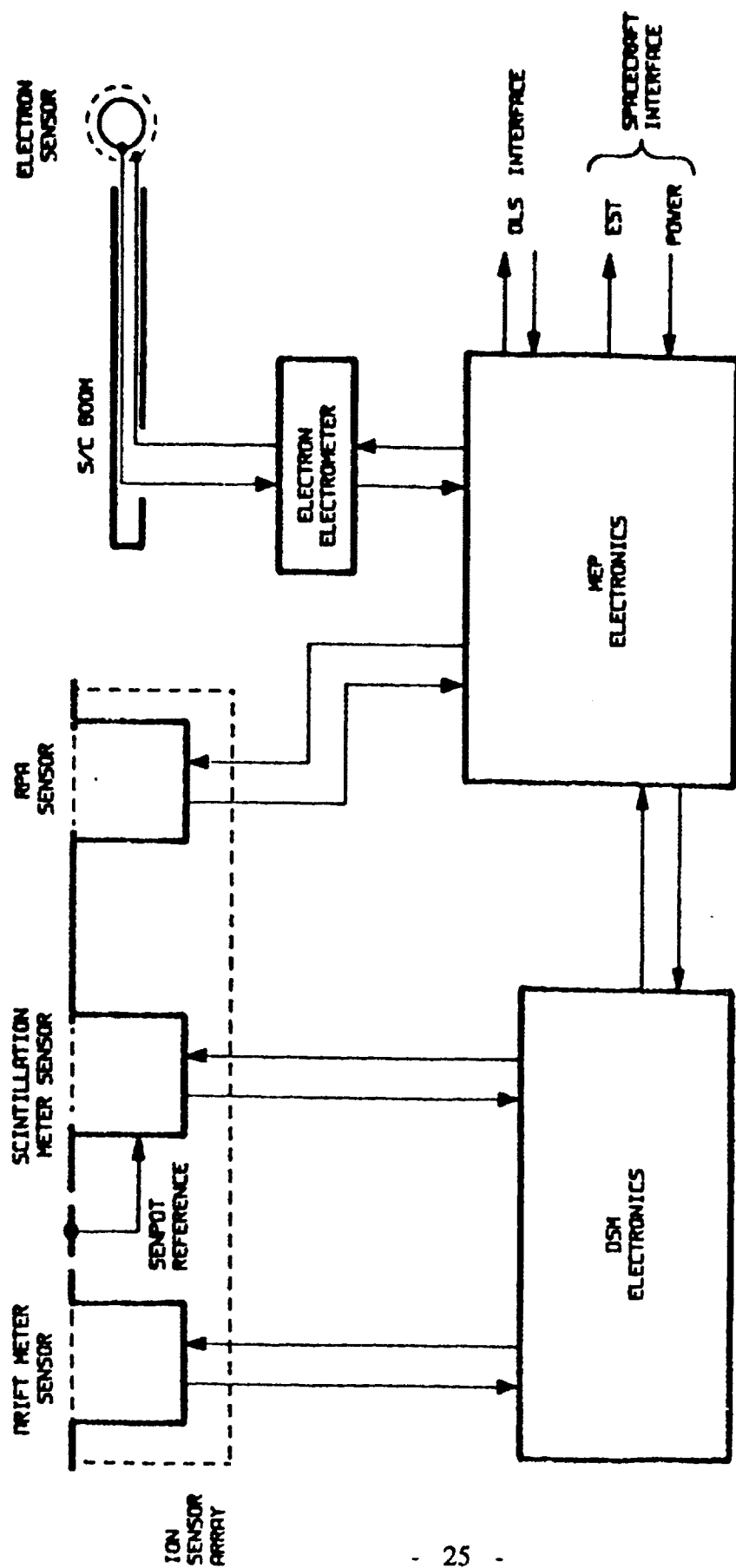
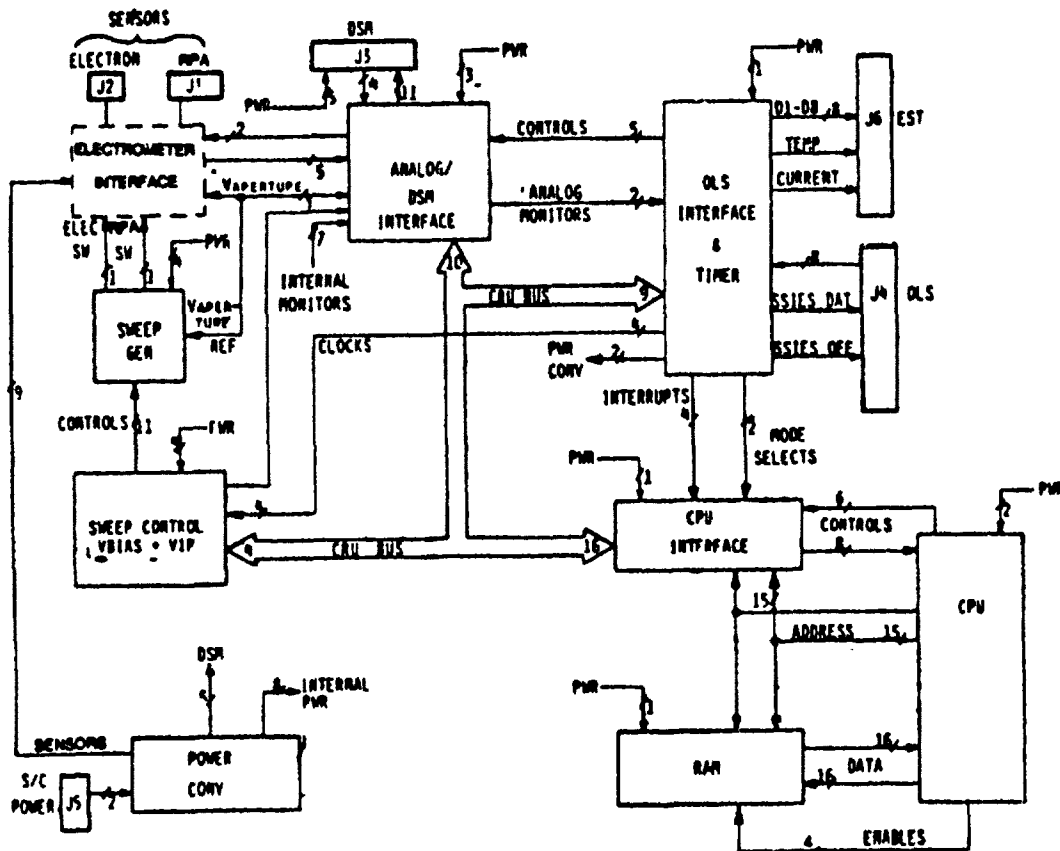


Figure 5-1 SSIES-2 Major Components

**Figure 5-2 SSIES-2 MEP Block Diagram**



NOTE: NUMBERS ON LINES REPRESENT QUANTITIES OF SIGNAL FUNCTIONS, AND ARE LOWER THAN THE ACTUAL WIRE COUNT. REFER TO SHEET 1 OF EACH SCHEMATIC FOR PRECISE WIRE COUNT.

The Electrometer Interface board (A1) is the interface to the RPA Sensor and to the Electron Electrometer. This board contains no active circuitry and is used only as an interface to the Electrometers.

The Analog/DSM board (A2) provides a dual function of analog data conversion and interface with the DSM. The analog function provides 16 channels of analog signal multiplexing as well as conversion to nine bits of digital data. The DSM interface routes four timing clocks and seven control lines to the drift meter and receives three analog signals which are converted for downlinking. The Analog board also contains two regulators that provide power to the DSM.

The sweep generator (A3) provides the necessary periodic waveforms for biasing both sensors. The sweep generator ramps are actually staircase waveforms with very small steps. This requires use of Digital-to-Analog Converters (DACs).

The implementation approach of using integrated monolithic 12-bit DACs eliminates discrete circuitry requiring greater board area. Included here are up-down counters to sequence the DACs as required. All control inputs to the sweep generators come from the backplane while outputs are routed to the sensors via the log amplifier board.

The sweep control and bias board (A4) provides control outputs to the sweep generator board based on inputs it receives from the microcomputer. Since both sweeps are referenced to biases, a level shifting function is provided via opto-isolators. The selection of opto-isolators rather than discrete transistor or transformer techniques provides a density advantage. The control outputs select ramp direction, rate, and inhibit functions available on the sweep generator board. In addition, the basic system electron bias,  $V_{bias}$ , is generated on this board from microcomputer control information. This implementation is again an integrated DAC as opposed to a less-dense discrete approach. A second DAC control voltage is added to provide the basic RPA system bias of  $V_{bias} + V_{IP}$ .

The OLS interface board (A5) provides both system timing functions and interfaces to the Operational Linescan System (OLS) command and data functions. The timer function utilizes the OLS reference clock to generate sweep clocks and synchronize analog-to-digital conversions. Processor control of this timing is also implemented to select and synchronize MEP operation with RED (OLS readout) pulses. A receiving register is provided to accept OLS serial commands, and register states are buffered as outputs of command receipt status. The basic serial data stream, read out in bursts by

the one second period RED pulses, is serialized on this board and shifted out. Major tradeoffs on this board relate to how much of each function is controlled by the processor versus hardware. Command receipt and data interfaces have been designed for maximum flexibility by allowing the processor, rather than dedicated hardware, to interpret data.

The CPU interface board (A6) interfaces the boards described above to the Central Processing Unit (CPU). To accomplish this, the interface translates the CPU medium-speed Communications Register Unit (CRU) bus to a set of inputs and outputs compatible with other boards. Data outbound from the processor is output in a serial NRZ-L signal with an associated clock. One of a number of strobe pulses is activated to complete the data transfer with a specific destination function.

For data inbound to the CPU, a data selector function is provided that works in conjunction with address bits on the backplane to read data into the CPU on a serial NRZ-L line.

CPU interrupts are acknowledged on this board and provision is made for resetting them under processor control. In addition, spacecraft pulse discrete commands are interfaced to the processor.

The RAM board (A7) provides all random-access read/write memory requirements for the CPU. On this board, 16,384 16-bit words of CMOS memory are available to the processor. This memory has been selected over the nearest contender for its superior combination of radiation-resistance, low power, and density. Density of the device is a four-fold improvement over previously available CMOS devices.

The CPU board (A8) contains the processor and 6,144 16-bit words of Programmable Read-Only Memory (PROM). Provision has been made for an additional 2k words of memory, but these devices have not been installed on existing units. An oscillator is also provided to furnish the required processor clock.

The power converter subassembly consists of four boards (A9-A12). The top three boards are all secondary regulators while the bottom board provides the basic power converter input filters, front end ON/OFF control, buckswitcher, and DC-to-DC converter. This subassembly is in a shielded compartment to minimize noise.

### 5.3 Unit Characteristics

The MEP has been partitioned into functionally complete elements which comprise the printed circuit board assemblies within the unit. The sections following describe the individual functions accomplished by the boards or, in the case of the power converter and sweep electronics, by a subsystem constituting several boards.

#### 5.3.1 Sweep Subsystem

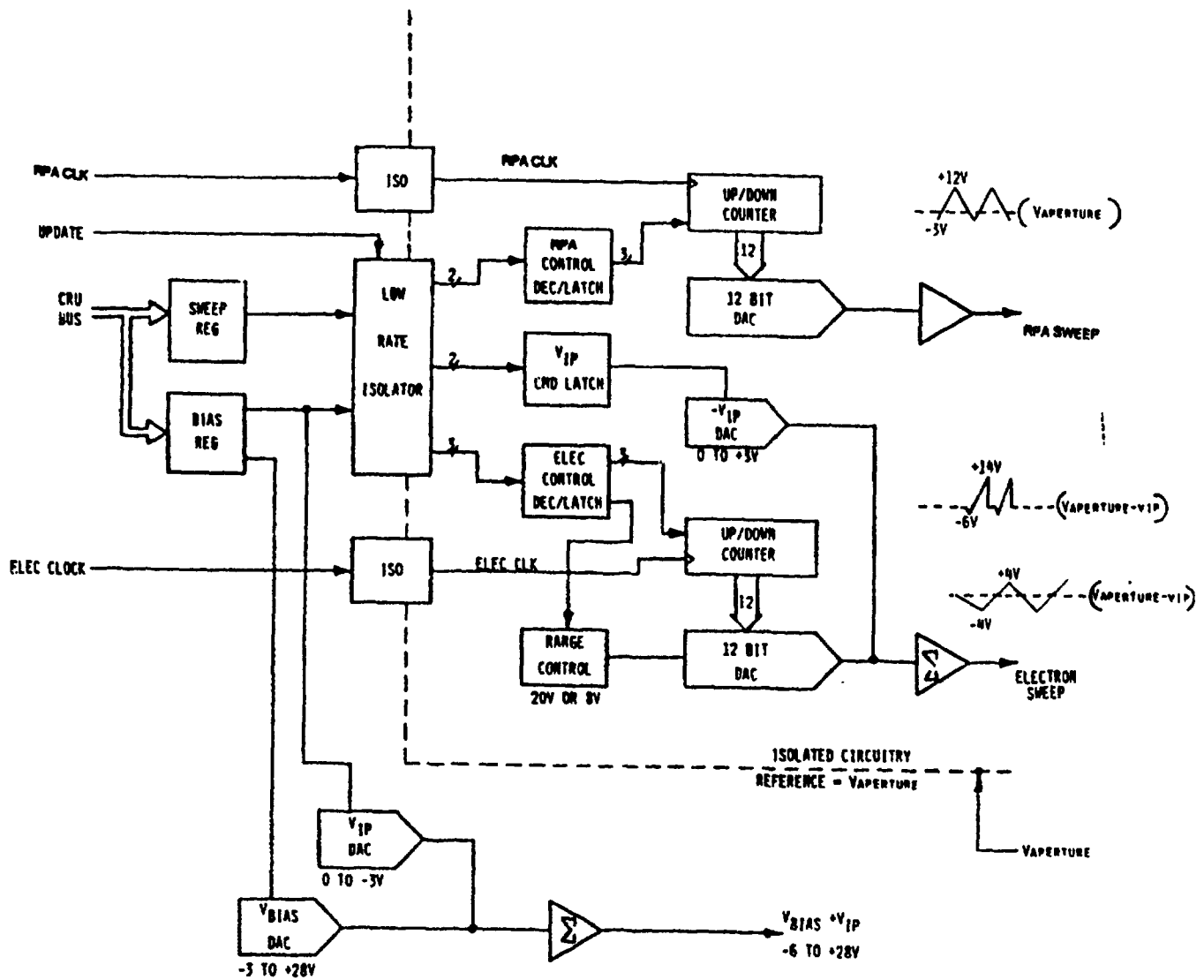
The sweep subsystem depicted in figure 5-3 is a consolidation of two printed circuit boards, the sweep generator and the sweep control/Vbias, used to produce a total of three programmable bias voltages. One voltage,  $V_{bias} + VIP$ , is a DC bias voltage which may be set, under processor control, to any one volt step within the range of -3 volts to +28 volts. The other two outputs are DC isolated sweep generators, which are return referenced to the  $V_{bias} + VIP$  output.

The sweep generator board contains 12-bit binary up/down counters, D/A converters, summing amplifiers, and a precision reference. These components are used to produce the two sweep outputs shown in figure 5-4.

The RPA sweep is a staircase of 3.75mV steps, occurring at 1ms intervals, starting at -3V, increasing to +12V, and then reversing direction to return to -3V. The total time for each complete up/down cycle is approximately eight seconds. The ELECTRON sweep is a similar staircase function with some additional programming flexibility. The normal sweep range is from -4V to +4V with respect to  $V_{bias}$ . It is important to note, however, that  $V_{bias}$  is not a measurable output, but is a reference voltage equal to the RPA sweep reference offset by VIP, a DAC controlled bias generator.

All programmable bias supplies and sweep outputs are produced by high-precision digital-to-analog converters with current outputs. As a result of this implementation, and the fact that not all currents are immediately converted to voltages, certain voltage offsets, such as VIP, are not available as direct outputs, but instead are summed at the bias buffer amplifier inputs. Elimination of this extra step of voltage conversion minimizes the error contributions to the final output voltages. Additionally, the high resolution of the sweep DACs provides for a very smooth ramp

**Figure 5-3 Sweep Sub-system Block Diagram**



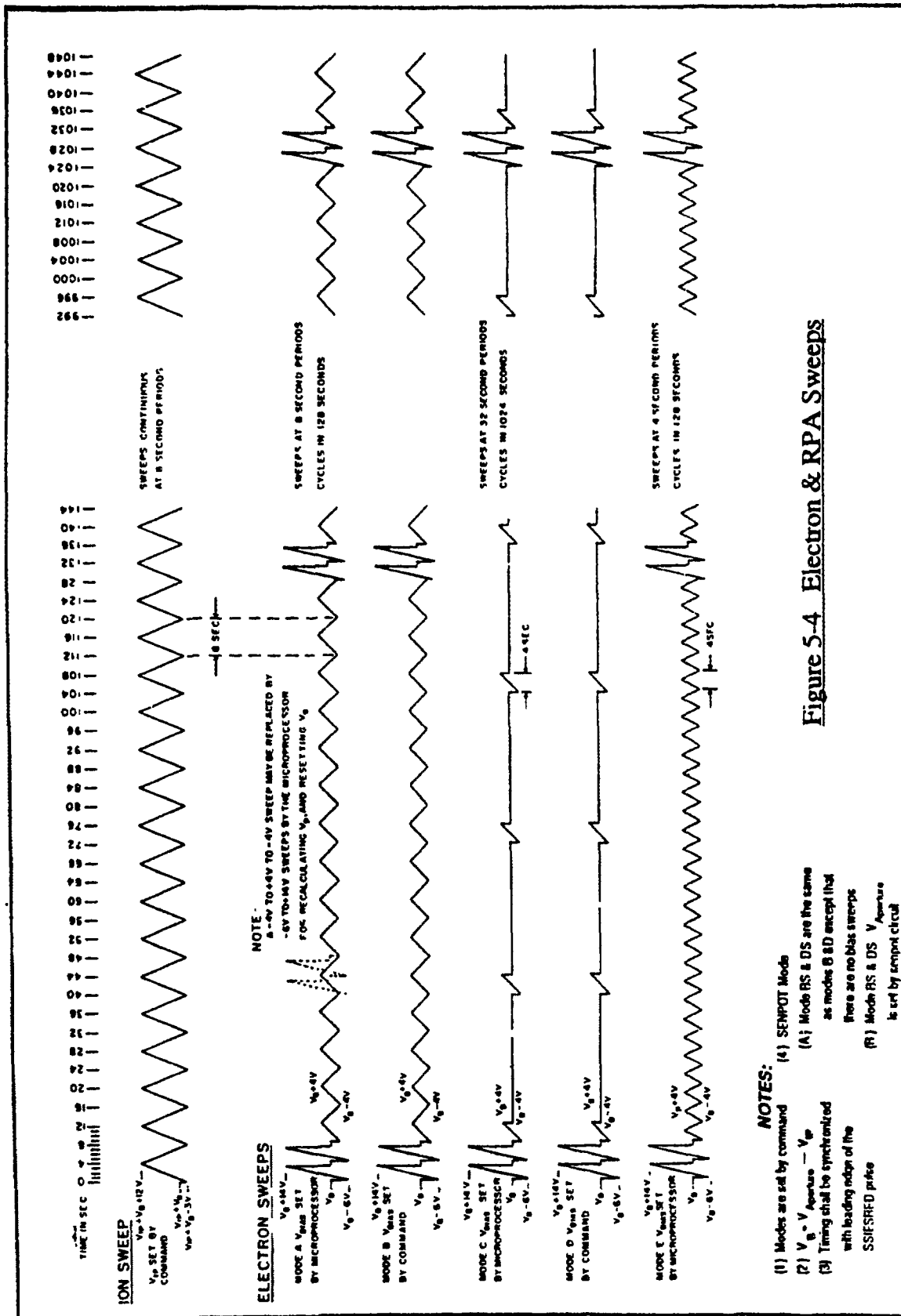


Figure 5-4 Electron & RPA Sweeps

- NOTES:
- (1) Modes are set by command
  - (2)  $V_p = V_{max} - V_{min}$
  - (3) Timing shall be synchronized with leading edge of the SSIFERED phase
  - (4) SENSITIVITY Mode
  - (A) Mode RS & DS are the same as mode B & D except that there are no bias sweeps
  - (B) Mode RS & DS  $V_{max}$  is set by sweep circuit

function, with 2mV/ms steps for the ELECTRON sweep, and 3.75mV/ms steps for the RPA sweep output.

A special bias setting sweep may be enabled by the processor to assist in the setting of  $V_{bias} + V_{IP}$ . During this operation the ELECTRON sweep output voltage is increased to cover a range of -6V to +14V. This is accomplished by temporarily enabling a higher DAC reference current input. Since the selected converter is a multiplying type, a current increase by two and one-half results in a total output range of 20V (instead of 8V). Additional offset current is introduced at the summing amplifier to move the starting point of the sweep down to -6V.

The sweep control/ $V_{bias}$  circuit is directly associated with the sweep generator. It comprises CRU bus update latches, opto-isolators, and latched control decoders, which provide all necessary isolated signals for electron and RPA sweep operation.

Control of the sweep generators is accomplished by sending control words to an 8-bit update register. The processor must refresh this data as often as once per second depending on the desired function. Two bits of this word are decoded for RPA sweep operation, providing four control functions as follows:

- (1) ZERO - pulses ZERO R to start sweep at 0V, but turns CLK R off, stopping the sweep
- (2) NO-OP - no change in present control
- (3) UP - pulses RESET R to start sweep at -3V, sets sweep direction to UP, and turns CLK R on, starting the sweep
- (4) DOWN - sets sweep direction to DOWN.

Since the control functions described above are decoded in the isolated section of the circuit, the decoder input bits are transferred across opto-isolators, and loaded into a latch by UPDATE, a TIMER generated signal occurring with every RED pulse. Due to the large power demands of the opto-isolators, with input signals present, and UPDATE GATE signal is provided by the TIMER to enable the isolator inputs only for a time sufficient for UPDATE to operate.

Electron sweep bits are handled in a similar fashion, except that three bits are used to provide the following five control functions:

- (1) ZERO - pulses ZERO E presetting sweep to 0V, selects -4/+4V sweep, and turns CLK E off, stopping sweep

- (2) NOP - no change in present control
- (3) BIAS - pulses START E resetting sweep to -6V, selects -6/+14V sweep, sets sweep direction to UP, and turns CLK E on, starting sweep
- (4) UP - pulses START E resetting sweep to -3V, selects -4/+4 volt sweep, sets sweep direction to UP, and turns CLK E on, starting sweep
- (5) DOWN - sets sweep direction to DOWN.

Sweep clocks for both generators are continuously provided from the OLS/Timer board, and are passed across the DC isolated interface to the sweep generator by means of two high-speed optocouplers. Normally, these devices are clocked at a 1kHz rate, although the electron sweep clock rate is increased to 2kHz during Mode E.

### 5.3.2 OLS Interface and Timer

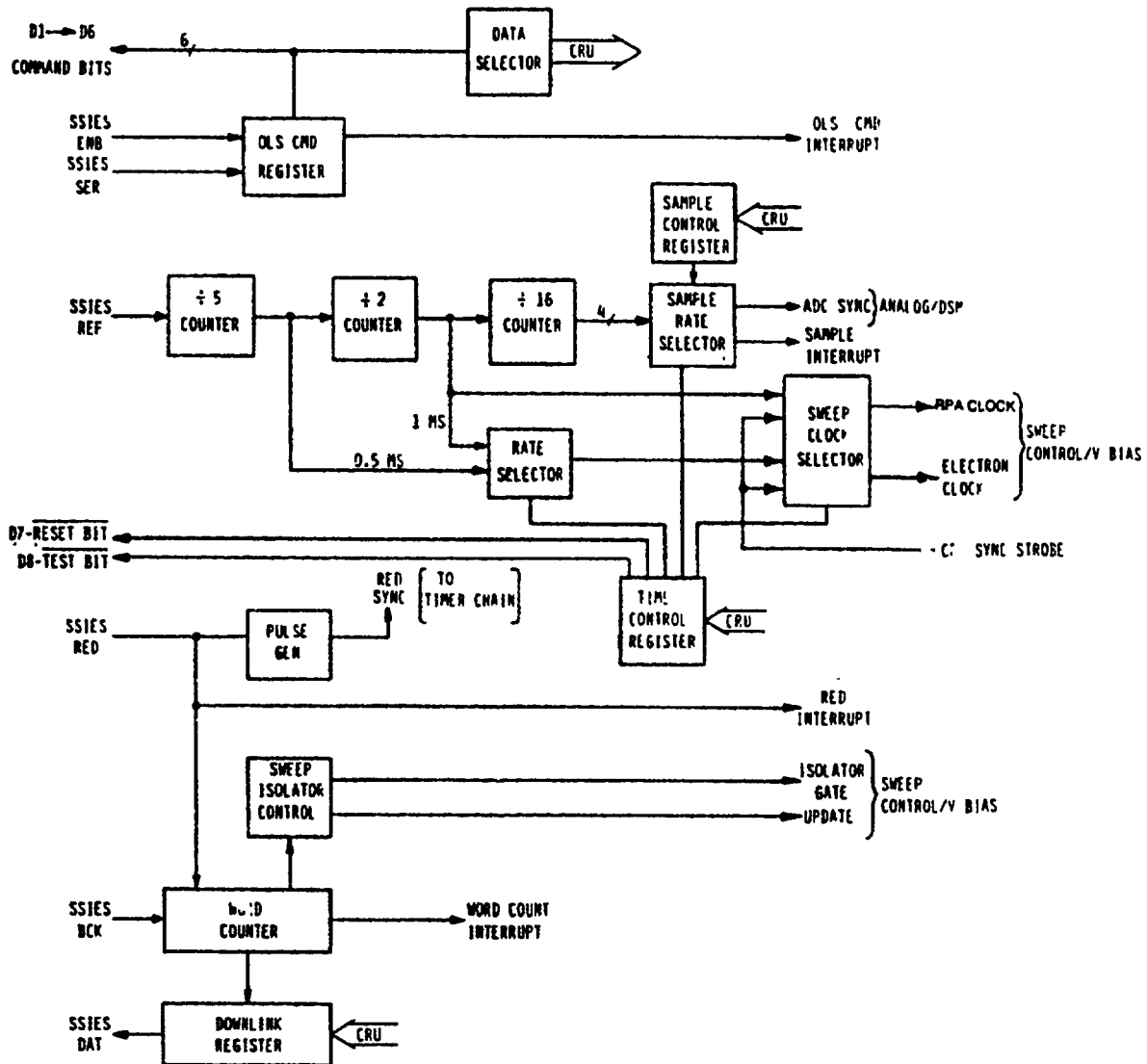
The OLS interface and timer, shown in figure 5-5, integrates a variety of functions on a single printed circuit card. The following four basic functions are included:

- (1) Controls all communication with the OLS
- (2) Generates telemetry output to the EST signals
- (3) Generates and distributes timing and control signals for MEP and DSM operation
- (4) Accepts the single point system ground reference (data return) from the OLS.

CMOS logic, powered by +5V, is used throughout, to implement the above tasks. This results in very low power consumption, an important system consideration. All input interfaces from unit connectors are protected from over and under voltages by diode clamp networks. In addition, these signals are buffered by Schmitt trigger stages to enhance noise immunity.

Communications with the OLS are divided into three categories: receiving timing information, receiving serial command messages, and transmitting formatted downlink data. The OLS sends a system clock, named SSIESREF, as a continuous (10kHz rate) stream, while once a second, synchronized bursts of 1080 similar clocks (SSIESBCK) are provided to facilitate the transfer of downlink data. SSIESRED is an envelope signal which has a duration equal to the length of each SSIESBCK clock burst. All MEP synchronous timing is generated from these signals. Serial command messages are received as SSIESSER, an NRZ-L data stream which must be interpreted using an associated command envelope signal (SSIESENB) to gate eight SSIESRED clock pulses. These board generated clock pulses, now synchronized

**Figure 5-5 OLS Timer Block Diagram**



with the incoming message, shift the command into a storage register and signal the CPU, by means of an interrupt request flag. The eight-bit command message will then be read by the CPU through a data selector, which enables one bit at a time to be transferred serially on the CRU bus to the processor for decoding and further action.

Downlink data transfer is also managed from the OLS/timer, in conjunction with the CPU. The SSIESBCK readout clock is counted and divided by nine to produce interrupt requests to the processor. A double-ranked, nine-bit data register allows synchronization of high-speed (10kHz) readout. The high-speed register is refilled every nine readout clocks, during the middle of a nine-bit word readout. At the end of each word readout, a load pulse causes an immediate and synchronous parallel transfer of a new word from the high-speed register into the low rate readout register, such that no interruption of the data flow may occur. Format control and primary storage of data is accomplished in the CPU subsystem, where accounting of specific data word numbers is maintained based on word count interrupts from the OLS/timer.

Delivering telemetry outputs to the EST is the second function of the OLS interface and timers. Six of the eight bits of the OLS command register are buffered out as parallel discrete-level indicators to the EST connector, and provide status of the last command message received from the OLS. Two additional discrete indicators identify reset and Uplink mode activity in progress. Analog monitors for temperature and current pass through this board on the way to the EST connector, but originate in the analog/DSM and power converter circuits respectively.

The generation of timing and control signals is a primary function of this board. Processor interrupts, analog conversion start pulses, sweep generator clocks, and special isolator control signals are all developed from OLS timing.

The following four types of interrupts are sent to the CPU subsystem to initiate further action:

- (1) OLS CMD INTERRUPT - asserted, asynchronously with respect to SSIESRED, whenever an OLS command has been received, but polled by the CPU
- (2) WORD COUNT INTERRUPT - produced at the end of the fifth bit clock of each nine-bit data word, during readouts, to request the processor to send the next word for downlink

- (3) RED INTERRUPT - produced at the leading edge of every SSIESRED envelope, and used by the CPU to generate seconds timing
- (4) SAMPLE INTERRUPT - produced by dividing the SSIESREF clock to develop four clock rates, of 1, 2, 4, and 8ms. One of these four rates is selected according to the contents of an eight-bit data word in the sample control register. The CPU responds to this interrupt by taking conversion data from the analog/DSM board and sending it a new sample address.

In close association with the sample interrupt, the OLS/timer sends analog conversion start pulses (ADC SYNC) to the analog/DSM board, at event intervals, midway between interrupts. This allows for long multiplexer settling time before a new analog sample is processed. In addition, this timing is synchronized with sweep generator clock timing, to minimize bias voltage disturbances during analog conversions.

Sweep generator clocks are developed from the same counter chain as the interrupts. A 1ms rate pulse is normally sent to both the electron and RPA sweep generators, but additional control may be commanded by the CPU. The clocks may be disabled, or a substitute clock, CPU SYNC STROBE, may be used during sweep calibration, to meter out a specific number of clocks. Another control can double the rate of electron sweep clocks, as required by Mode E. These actions are activated by control bits from a data word contained in the timer control register, and can be immediately updated by means of a CPU instruction, as necessary. This register is also the source of the reset and uplink/test mode flags, and a CYCLE 1 I.D. bit used with SSIESRED to produce the CYCLE 1 clock required by the DSM.

Special isolator control signals, to provide low-power updating of sweep control registers, are generated once per second. Timing is developed from the divide-by-nine word counter at the beginning of each second. An ISOLATOR GATE enable signal is sent to the sweep control board for a total of 500us, to energize the optocoupler diodes. During this period, an UPDATE pulse strobes this information across the DC isolated interface to the sweep generator board.

This last function of the OLS interface and timer board is to provide the entry point into the SSIES-2 system of the OLS data return. The data return line is used as the single point of reference for all analog and digital voltages

within the system, and attaches to the MEP backplane ground system at the OLS/timer. All other secondary grounds ultimately return to this point.

### 5.3.3 Analog/DSM Interface

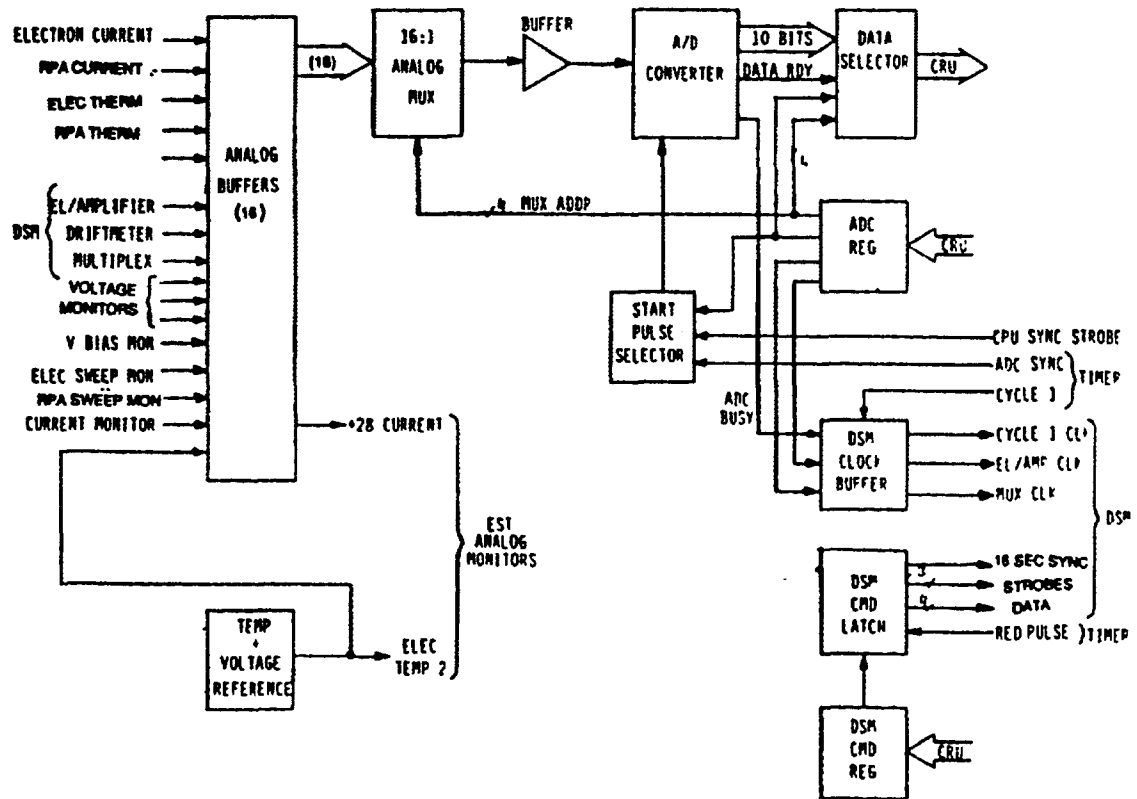
The Analog/DSM interface circuitry consists of two major functions with a certain amount of overlap, as shown in figure 5-6. The analog portion contains an A/D converter with a 16-channel input multiplexer and a microprocessor interface. The DSM interface is an eight-bit parallel latch, with buffers and a microprocessor interface, and additional buffers for special timing outputs. Also, a monitor circuit is included as an analog indicator of unit temperature.

Sixteen analog input buffers, in a voltage follower configuration, accept signals from many sources, including:

- (4) RPA and Electron Sensor Electronics outputs
- (3) DSM unit outputs
- (9) Internal signals and monitors

Two eight-channel CMOS analog switches select one of 16 inputs for conversion. Their outputs are buffered by another precision op- amp (OP-15), to drive the relatively low impedance input of the A/D converter. Common mode range considerations constrain the useful range of inputs to a low of roughly -3V and a high of +8V. The bipolar input range of the A/D converter (-5.1V to +5.1V) further reduces the full performance range to -3V to +5.1V, which is represented as a 10-bit output (1-bit sign + 9-bits magnitude). The A/D converter uses I<sup>2</sup>L technology, and may be operated by either the TIMER or CPU, upon receipt of a synchronization pulse. The TIMER generates ADC SYNC for this purpose, while CPU SYNC STROBE is a CRU-bus dedicated strobe which accomplishes the same end.

Figure 5-6 Analog/DSM Board Block Diagram



A software-controlled latch is loaded by the CPU with an eight-bit word, containing a bit for selection of the synchronization pulse source, four bits of multiplexer address, and additional select bits for DSM interface clocks. These data bits are also directed to the output data selector for possible retrieval by the CPU, if analog function status is required.

In normal operation, the CPU sends an eight-bit word containing the address of the next analog sample desired, and the source of the synchronization pulse to be used as a start. This allows for immediate selection of the appropriate input buffer, to avoid switch settling problems. Upon receipt of the synchronization, the DAC processes the input voltage (in approximately 25us) and latches the result, along with a data ready flag, for subsequent readout by the CPU via the output data selectors. The CPU repeats this cycle by sending the next sample address after it has obtained the previous data.

The temperature monitor circuit provides an analog indication of unit temperature to the EST monitor and is also sampled by the A/D converter, one of several system temperatures to be digitized and downlinked with other system data. A voltage reference device (REF-02) with a unique linear temperature output is used to provide a 2.1mv/°C characteristic. This signal is amplified and level shifted by an additional amplifier stage to produce a 0-5V indicator, which, when digitized, produces steps of approximately 40mV (4 LSB) per degree.

When samples of either EL/AMP or MULTIPLEX inputs from the DSM are required, an appropriate select bit is included in the control word sent to the DAC control latch. These bits are used to enable sample clocks, generated by the A/D conversion period (25us). The two resultant clocks, EL/AMP CLOCK and MULTIPLEX CLOCK, are buffered, along with a timer-generated clock (CYCLE1 CLOCK), out to the DSM system. The remainder of the DSM interface consists of an eight-bit buffered command latch. The CPU directs DSM/OLS command messages to the command latch. All eight latch outputs are buffered out to the DSM connector and are diode protected.

### 5.3.4 CPU Subsystem

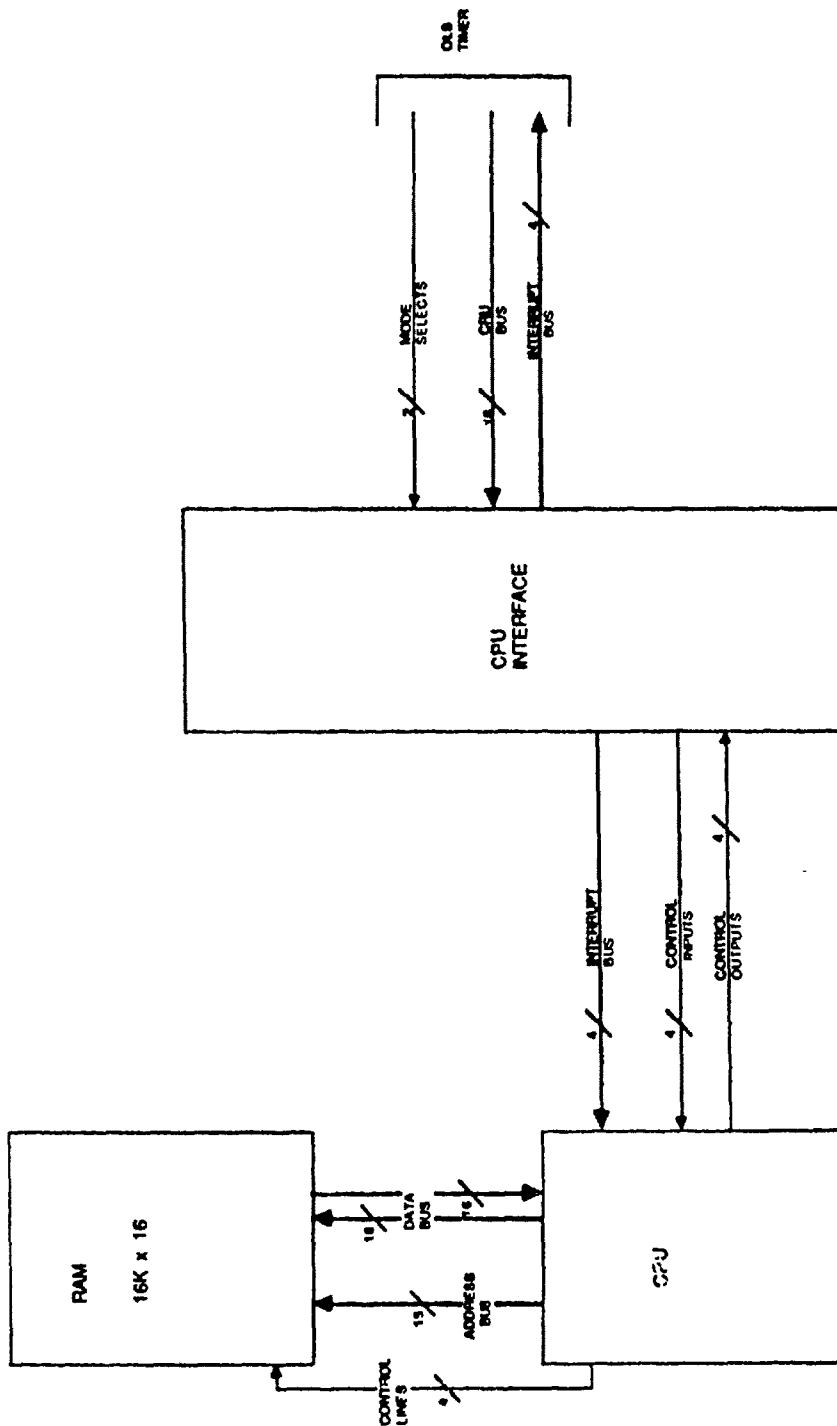
The Central Processing Unit (CPU) subsystem contains the microcomputer, memory, and all interfacing necessary to connect the CPU function to the backplane. As shown in figure 5-7, the subsystem is partitioned into three circuit boards: CPU, RAM, and CPU interface.

The CPU board shown in figure 5-8 has a microcomputer (SBP 9989) and PROM (HM6616) as its basic elements. In the PROM will reside a stored program and tables for logarithms. The PROM is organized as two banks of 2K words x 16 bits. This program will perform control functions for the system, as well as RPA and electron calculations.

The processor is also capable of accepting an uplinked program to run in place of the on-board prom program. Hardware and PROM firmware have been implemented to allow the necessary bank switching, synchronization, and error checking for this process to occur. The CPU board has its own 1MHz clock, which is independent of (and asynchronous to) other system clocks. The processor subsystem is interrupt driven by a set of prioritized interrupts that come from the CPU interface board.

The SBP9989 executes the correct interrupt routine based on the internal mask. The SBP 9989 has a serial method of doing I/O using an internal CRU. When performing an output instruction, the CPU produces a clock, serial data, and an address for each bit of data sent. After each bit is sent, the CRU address is incremented. The processor is capable of sending from 1 to 16 bits of sequential data during each CRU instruction.

Figure 5-7 CPU Section Block Diagram



AFGL SSIES-2  
CPU SECTION BLOCK DIAGRAM

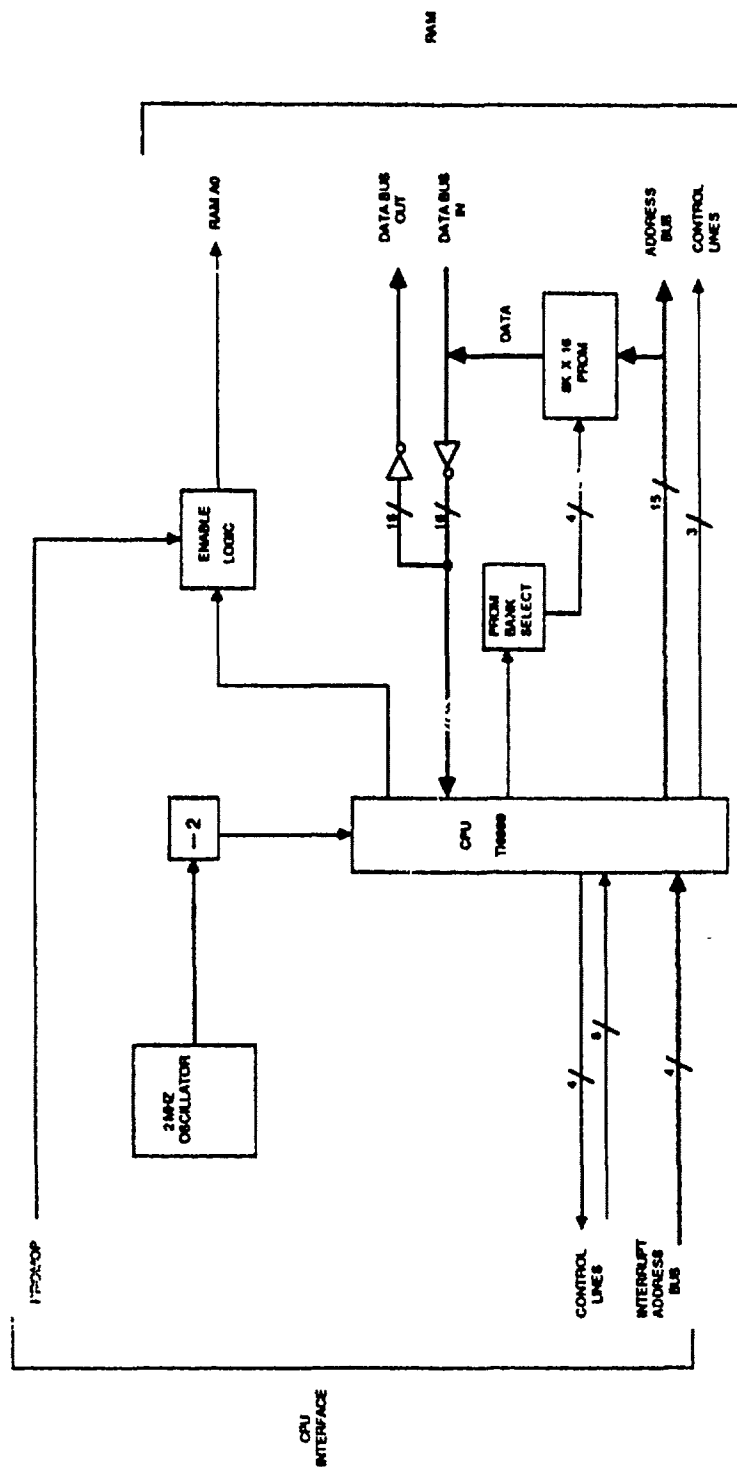
Date: March 2, 1987 Sheet 1 of 1

ANALYTIX DRAWING NUMBER: 2502

**analytix**

A Sanders/Lochhead Company

Figure 5-8 CPU Block Diagram



AFGL SSIES-2  
CPU BLOCK DIAGRAM

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Date: March 2, 1987

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A Sanders/Lochhead Company

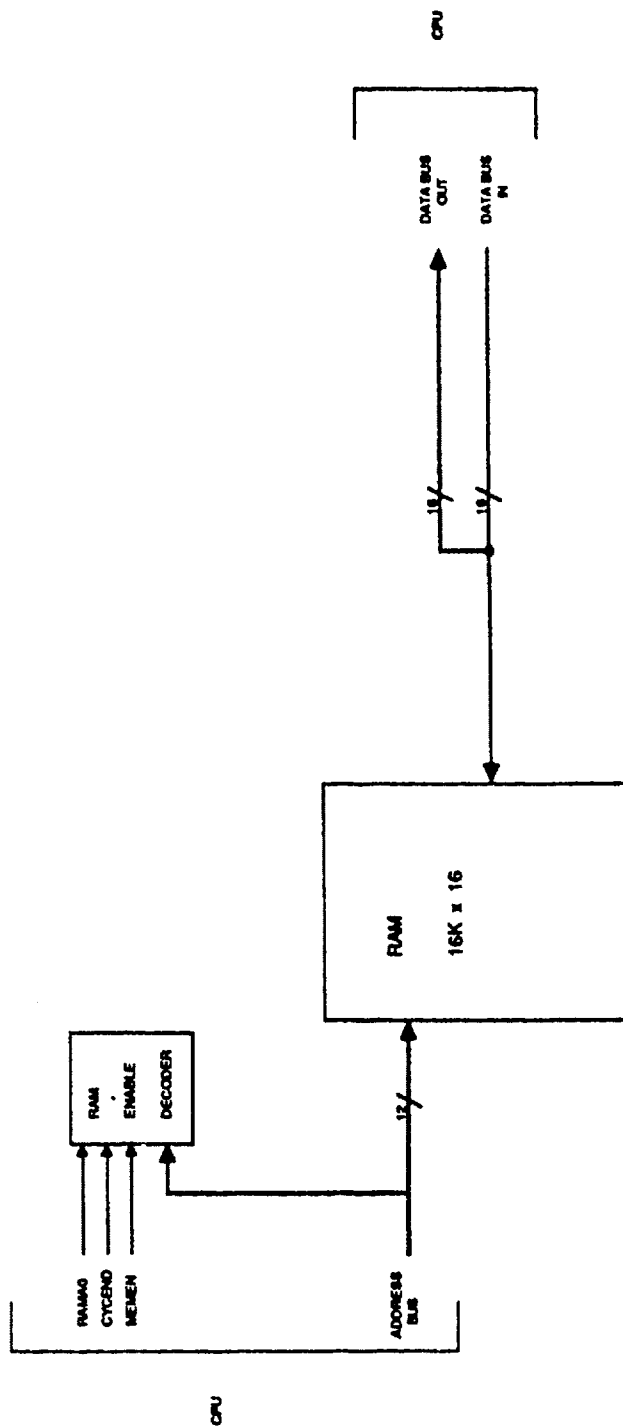
The RAM board, shown in figure 5-9, contains the volatile memory for the system. Registers, intermediate values, flags, pointers, address locations, and the final data to be downlinked to earth are stored in the RAM. The RAM board is configured in banks of 4024 x 16. This complement of memory was used in order to facilitate block loading of a program of about 3 times the present length. With the present version of Prom code having a duty cycle of less than 20%, this larger Ram space allows significant program enhancement capability, both in the length of code and execution time.

The CPU interface board shown in figure 5-10 serves three functions: first, it acts as an interface between the CPU section and the rest of the SSIES-2 system; second, it controls the bank switching and reset circuitry; and third, it latches and decodes interrupts.

The CPU interface board makes use of the SBP 9989 CRU system for I/O. The CRU is a serial method of performing I/O developed by TI. Control circuitry on the CPU interface board provides all the added control signals necessary to operate the "CRU BUS". Bank switching and reset circuitry are important functions of the CPU interface. Bank switching is a processor initiated function that allows the Ram to be re-mapped to the Prom address space. This is essential for the block loading of files.

The CPU interface board controls the latching of interrupts and Interrupt Request generation. The interrupt reset decoder resets interrupts on processor command.

Figure 5-9 RAM Block Diagram



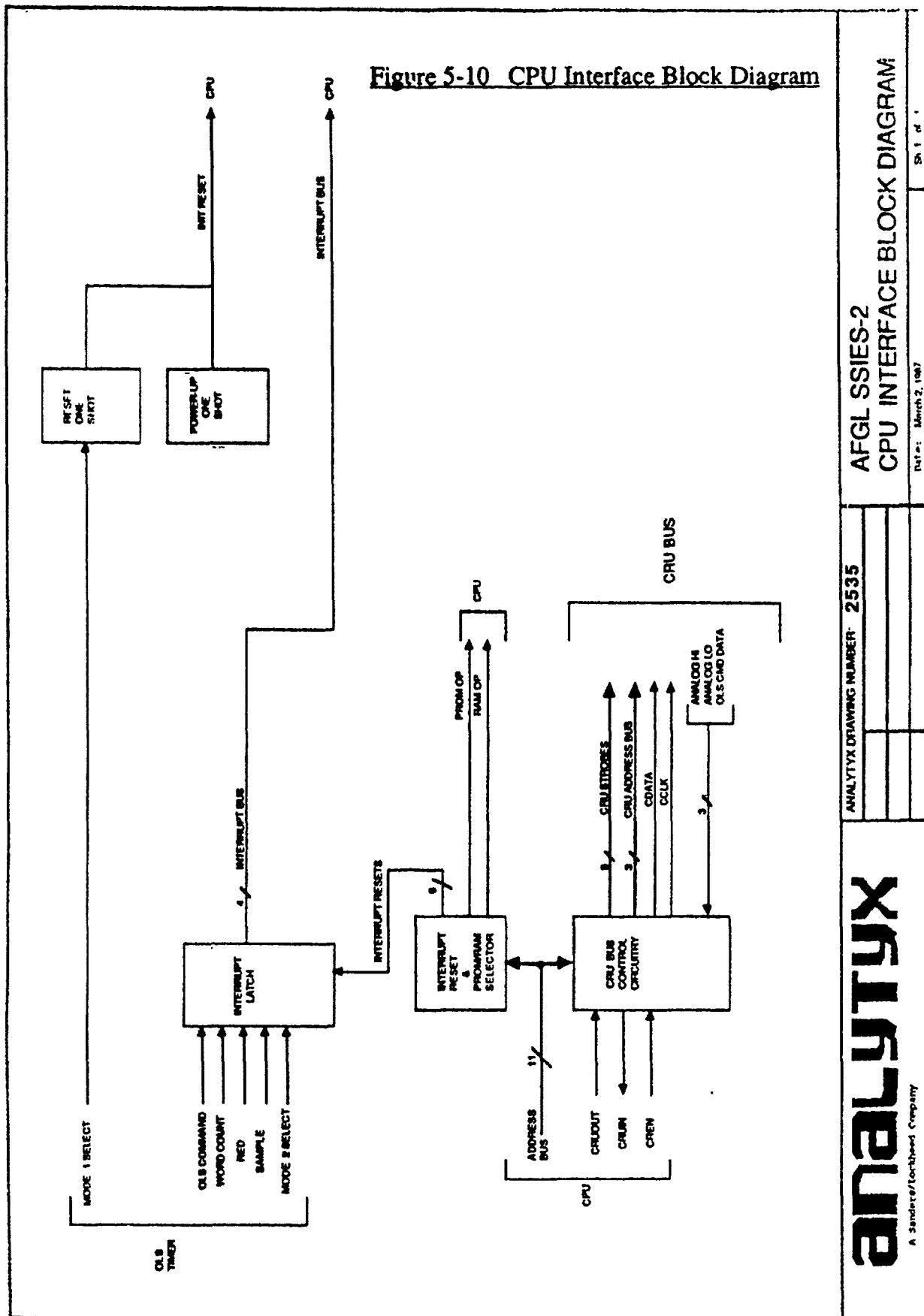
AFGL SSIES-2  
RAM BLOCK DIAGRAM

ANALYTIX DRAWING NUMBER: 2541

Date: March 2, 1987

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**analytix**



## **5.3.5 Power Converter and Power Requirements**

### **5.3.5.1 Power Converter**

The main purposes of the regulator- converter are three-fold, as follows:

1. **Power Conditioning** - Converts the single main 24 Vdc to 32 Vdc power bus to multiple isolated DC voltages
2. **Regulation** - Regulates the output voltages against changes in input line voltage or output load variation
3. **EMI Control** - Protects the outputs from transients and audio range to high frequency variations of the input power bus

In addition to the above, the conversion process must not emit adverse RFI of its own.

The power converter block diagram is depicted in figure 5-11 and consists of an inrush current limiter, input filter, buckswitcher DC/DC power converter, and output regulators.

As the block diagram shows, dual regulation is utilized to satisfy the constraints of the imposed specifications; i.e., the input high-efficiency regulator pre-regulates out the wide input line swing thereby minimizing the voltage drop across the less- efficient linear output regulators. In turn, the linear regulators compensate for load and temperature variation, and provide regulation isolation between the system components, therefore eliminating crosstalk.

### **5.3.5.2 Power Requirements**

The total input +28V power requirement is typically 10W. The 12W power budget of the MEP provides a comfortable design margin.

```

graph LR
    JA[JA] -- +5V --> CL[BULKY CURRENT LIMITER]
    JA -- CABLE GROUND --> CL
    CL -- POWER RETURN --> JA
    CL -- 55SEEPEN --> R[R]
    CL --> IF[INPUT FILTER]
    IF --> BS[250KZ BUCKSWITCHER]
    BS --> DCDC[250KZ DCDC CONVERTER]
    DCDC --> MEP[MEP]
    DCDC --> DSM[DSM]
    DCDC --> OFE[OFE]
    MEP -- 8 SECONDARIES --> MEP_OUT((MEP))
    DSM -- 2 SECONDARIES --> DSM_OUT((DSM))
    OFE -- 7 SECONDARIES --> OFE_OUT((OFE))
    OSC[250KZ OSCILLATOR] --> BS
    OSC -- POWER ENABLE --> CL
    OSC -- POWER ENABLE --> DCDC
  
```

**Sanders / Lockwood Company**

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Date: March 2, 1997

### 5.3.6 Description of Firmware Program

The operation of the Main Electronics Package is controlled to a large extent by the program executed by the microcomputer. This program, stored in Programmable Read-Only Memory (PROM), is categorized as interrupt processing, electron data processing, ion data processing and block load processing.

#### 5.3.6.1 Interrupt Processing

Demands for the processor to accomplish a task are made by signals called interrupts. Interrupt signals direct the processor to execute a particular program segment called an interrupt service routine. Interrupts are assigned unique priority levels that establish what order the interrupt routines will execute if more than one interrupt is active at a time. The MEP has five interrupt routines with five different priority levels.

First, there is the RESET routine. This routine is the executive for the program. The routine loops and waits for an interrupt to request service. After an interrupt routine has finished all the necessary processing, the program control returns here to wait for the next interrupt.

The highest priority maskable interrupt is the INIT interrupt. The INIT routine is executed on power up, when either a discrete or serial Reset command is issued from the spacecraft or OLS, and when a Restart command is issued. INIT does a check on all RAM, clears all of RAM, initializes RAM memory locations, checks the state of the Senpot Relay, and initializes the hardware. The routine takes about 11 seconds.

The second highest priority interrupt is the RED interrupt. This interrupt occurs on one-second intervals as determined by the OLS System. The interrupt service routine controls the sweeps, decides when to call RPA (Retarding Potential Analyzer) and Electron processing routines, keeps track of the mode and seconds count, and initializes and resynchronizes the Sample interrupt.

The third priority interrupt is WORD COUNT. This routine sends data to the SSIESDAT shift register. In the course of shifting out 120 nine-bit data words, the interrupt is asserted for once for each word. The service routine takes each word from the downlink buffer and loads this word into the downlink shift register. Most of this data is a sample that was collected in the previous one second period. Figure 5-12 illustrates the downlink format.

The fourth priority is assigned to the SAMPLE interrupt. This interrupt is derived from the SSIESREF clock and occurs between each analog-to-digital conversion. Each time the routine is executed, the processor fetches the previous digitized sample, and stores the multiplexer address for the next sample.

The OLS interrupt, a software polled interrupt, indicates receipt of a serial command from the OLS subsystem. The service routine interprets the command and selects the appropriate routing or action. Commands can change the modes, sweeps, bias levels and other system characteristics for both the DSM and the MEP. Some of the commands are used in the block-loading mode for synchronizing.

The Test/Uplink interrupt, also a software polled interrupt, is used for either an uplink (block-load) or for a test mode. In the present system, this interrupt is used only for block loading, since no test modes exist.

Figure 5-12 Downlink Format

**SSIES - 2 DOWNLINK FORMAT**

MARCH 10, 1986

WORD	CYCLE 1 ID	CONFIG 1 ID	CMD MON OLS	CURR/INT MONITOR	RPA Thermistor	Vaperture MONITOR	RPA ION MONITOR	T <sub>H+</sub>	T <sub>O+</sub>	V <sub>P RPA</sub>	ELECTRON MONITOR	T <sub>E</sub>
1-12	CYCLE 2 ID	CONFIG 2 ID	CMD MON DSM	TEMP MONITOR	ELECTRON Thermistor	Bias MONITOR	SPARE	N <sub>H+</sub>	N <sub>O+</sub>	V <sub>SP</sub>	V <sub>P ELE</sub>	N <sub>E</sub>
13-24	RPA ION ..											
25-36	RPA ION ..											
37-48	DSM (ELE/AMP)											
49-60	DSM (DRIFT)											
61-72	DSM (Multiplex)											
73-84	DSM (ELE/AMP)											
85-96	ELECTRON ..											
97-108	ELECTRON ..											
109-120	RPA SWEEP						ELECTRON SWEEP					

PRR1 SSIES-2 FORMAT



PROPOSED REDUCTION IN DOWNLINK DATA

.. ION AND ELECTRON DATA CAN BE INTERCHANGED BY COMMAND

### 5.3.6.2 RPA Data Processing

The RPA data processing is performed every four seconds. The RPA processing procedure is invoked by the interrupt processing firmware when a new four-second set of ion raw data is available. The interrupt routines have already formed 100 double-precision values by first anti-logging and then summing five successive RPA log amp samples taken at 8ms intervals. The 500 samples at 8ms intervals span an entire four-second upsweep (-3V to +12V) or downsweep (+12V to -3V).

RPA processing firmware comprises six modules:

- (1) If downsweep data, reverse order of raw data buffer
- (2) Search for maximum linear delta in current
- (3) Search for the next largest delta
- (4) Determine which species are present
- (5) Perform two species calculations if needed
- (6) Perform one specie calculation otherwise

### 5.3.6.3 Electron Data Processing

Calculations on collected electron data are initiated every four seconds in Modes A-D and every two seconds in Mode E. Modes A-D acquire 96 data samples before calculating while Mode E acquires only 48. Electron data is smoothed during calculations as a result of the use of five-point straight line approximations during slope determinations.

First, minimum and maximum values are determined so end regions which are not of interest can be discarded. An initial horizontal line is fitted to the first five points. Then successive straight line fits are made and the maximum slope found. The intersection of the maximum slope line and the horizontal line yields information to allow computation of  $V_p$  (electron). The maximum slope also allows computation of the electron temperature. The electron density result is calculated in the logarithmic domain from the slope information and the projection of the intersection point onto the y-coordinate (log amp voltage) axis.

As in RPA processing, all results are stored in RAM memory where they are available to the SSIESDAT data output of the experiment.

### **5.3.7 Block Loading**

Block Loading is performed on command from the ground. During Block Loading, all other SSIES-2 functions are stopped and the microprocessor devotes all of its time to receiving a new program from the ground. During this time all interrupts are disabled while the processor continually loops waiting for data from the OLS. If for any reason the data is interrupted or lost, the processor will timeout after 5 minutes and return to the PROM resident program.

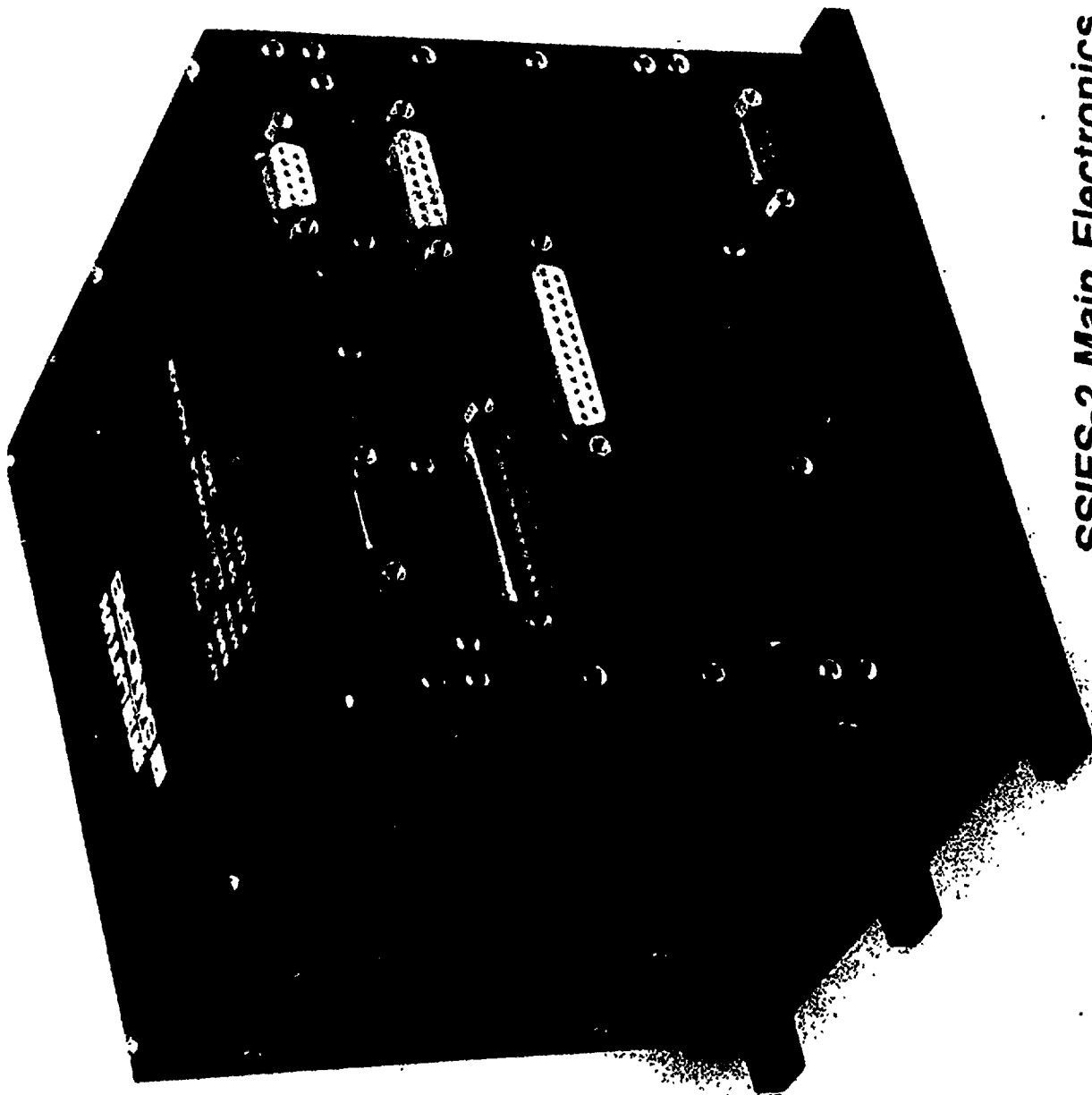
Block Loading allows the SSIES-2 to be reprogrammed in flight. This could be very useful for changing the algorithms to meet unexpected conditions, and to make improvements on the algorithms based on the SSIES-2 data.

### **5.3.8 Mechanical**

The SSIES-2 MEP is enclosed in a 6"X6"X6", 216 cubic-inch aluminum housing (shown in figure 3-11). These dimensions exclude mounting feet, external connectors, and hardware protrusions. The unit weighs 6.5 lbs. The mounting surface is finished with electrically conductive chemical film per MIL-C-5541, class 3. The remainder of the exterior surfaces are coated with Chemglaze Z306 polyurethane black paint. Six clearance holes have been provided at the mounting surface enabling the unit to be fastened to the spacecraft with number 10 hardware. External interconnect will be handled by rectangular type "D" style connectors J1 through J6 type D\*MA-NMB-K56 made by Cannon.

The MEP unit electronics are partitioned onto 12 multilayer, two-sided, .062 thick Printed Wiring Board (PWB) assemblies. There are three separable isolated sections; the log amplifier section, the power supply section, and the electronic stack section. The log amplifier PWB assembly is housed in a machined, single-piece aluminum structure that supports the board assembly and provides an external mounting surface for connectors J1 and J2, the RPA and Electron connectors that are part of the log amplifier assembly. The power supply section is made up of the primary buckswitcher/ TI-T2 transformer header PWB assembly, and three regulator PWB assemblies all mounted in a stack and fastened to the baseplate.

The power connector J6 is harnessed with a service loop and wired to the buckswitcher PWB. The electronics stack section is made up of a shield and a collection of seven PWB assemblies (the analog/DSM, sweep generator,



**SSI ES-2 Main Electronics Package**  
**AES Part No.: 2500      Serial No. 001**

sweep control, OLS interface, CPU interface, RAM, and the CPU) fastened together with male to female standoffs and mounted to the top of a machined, single-piece aluminum housing. The power connector J6 and the power supply section are installed in the bottom of this housing. The Electrometer interface section is mounted above the stack and fastened to the shield and two side plate/spacers that are fastened to the sides of the lower housing. An aluminum sheet connector plate to mount connectors J3, J4, and J5 is fastened to the lower housing, the shield, sideplates, and the log amplifier housing in front. On the back side of the unit, the three sections are tied together with aluminum sheet cover that, when removed, provides access to the systems backplane interconnect. The system interconnect is handled between the printed wiring assemblies and the backplane by Airborn 70 pin PC board and mating 80 socket cable connectors. Between the power supply and the backplane, a Cannon 50 pin rectangular "D" connector mates to a 50 socket rectangular "D" connector on the power supply.

The backplane is a flexible printed wiring assembly. The power supply is mounted on the baseplate with all "hot" components mounted remotely from printed wiring boards and heatsunk directly to the baseplate. In the upper compartment 0.24" hex brass spacers and strategic placement of "hot" components ensure improved reliability by lowering semiconductor and IC junction temperatures.

## **6. GROUND SUPPORT EQUIPMENT**

### **6.1 Introduction**

This section describes the characteristics of the SSIES-2 Plasma Monitor System Ground Support Equipment (GSE). A full GSE set consists of the a computer control system, a data acquisition rack system with custom interface electronics, and a set of associated flight test cables.

The information contained here is relevant to the S/N 001 & 002 Ground Support Equipment sets delivered, under sub-line item 0001AD, for support of SSIES-2 Plasma Monitor Systems. The Analytyx part number for these units is 59700-2630.

### **6.2 Unit Design Approach**

The Ground Support Equipment was designed to use up-to-date methods to provide power, command, sensor stimuli and data interfaces for the SSIES-2 Plasma Monitor Systems. Design goals included the addition of closed-loop testing, engineering units display, and memory block loading capabilities to those functions already available in earlier generation ground support units.

### **6.3 Unit Characteristics**

The GSE units consist of two major subsystems, a computer subsystem, and an associated electronics rack.

#### **6.3.1 Computer Subsystem**

##### **6.3.1.1 Computer System Hardware**

The computer controller used for the GSE system is a Hewlett Packard model 9816S/630. This 8 Mhz Motorola 68000 based workstation is a compact unit with a self-contained 9" CRT display. As configured, with a 1 Megabyte memory expansion board, a total of 1.25 Megabytes is available for operating system, program and data.

Communications are provided over three I/O ports. First, an HP model 98622A/001 (GPIO) parallel interface board is used to provide communications with the custom OLS interface board for commands and data. An internal RS-232 port is used for an external mainframe link, when independently developed block load programs are required to be sent to an SSIES-2 MEP unit. Finally, an IEEE-488 port is used for all other computer control of the dual disk drive unit, printer, or ACRO rack acquisition functions.

Test reports are printed on an HP Model 2225A Think Jet printer. This quiet and lightweight thermal ink jet printer is highly portable and convenient for transport to the environmental test facilities used for this program. All software and data is stored on 3 1/2 " microfloppy diskettes with a capacity of ~ 600 kbytes each.

#### 6.3.1.2 Computer System Software

Software for the GSE unit is divided into two categories, operating system and program. The operating system chosen for this application is the HP Basic Operating System, commonly referred to as Rocky Mountain Basic. This highly versatile realtime environment contains a unique function key driven structure, which is well suited to producing an operator friendly interface. Labels for up to 10 program functions are displayed on the CRT directly over the corresponding keyboard buttons. This is comparable to pull-down menus in operation, but does not require a separate pointing device. A hierarchical menu structure is employed for all GSE operations.

An important aspect of the GSE operating system is its hardware I/O capability. This HP computer is equipped with an IEEE-488 interface, and has high level commands available in BASIC to facilitate its use. The GPIO parallel interface is fundamental to the interrupt driven nature of the GSE, allowing for synchronization of timing between the flight unit under test and the GSE computer.

The operating program for the GSE provides many capabilities as summarized and categorized in the following list:

##### MEP Control Functions

- (1) MEP +28 volt Power ON/OFF
- (2) Power Enable (SSIESPEN) ON/OFF
- (3) Serial Commands (By Functional Name or Hex Value)

- (4) Discrete Commands (By Functional Name)
- (5) Block Load Commands (Manual or automatic modes)
- (6) Modify downlink format length (80 or 120 wds)

#### MEP Data Functions

- (1) Downlink Data - Raw Data Display (Hex or Decimal)
- (2) Downlink Data - Housekeeping Data Display (Engineering Units)
- (3) Downlink Data - RPA Data Display (Engineering Units)
- (4) Downlink Data - Electron Data Display (Engineering Units)
- (5) Downlink Data - DSM Data Display
- (6) EST Data Monitors - analog and digital
- (6) Buffer Downlink Data - 1024 seconds of any display

#### MEP Test Functions

- (1) Automatic Functional Test & Results Printout
- (2) Critical Parameter Monitoring (15 sec to 2 hour intervals)
- (3) MEP power bus - voltage & current monitors
- (4) MEP interface signals - analog voltage monitoring
- (5) Print Reports - tests or data buffer ranges
- (6) Test Data Storage - Operator, Location, Equipment IDs, Environment
- (7) Define Test Setup

#### Miscellaneous Functions

- (1) Clock/Calendar Setting
- (2) Comment Editor
- (3) Overcurrent / Overvoltage Alarm Controls
- (4) Block Load File Translation
- (5) View Data Buffer

The first category of commands is oriented toward controlling the SSIES-2 flight hardware, and allows for turning power on and off, as well as issuing commands or uploading programs. As with all functions, operator input is via the function keys ("softkeys" in HP terminology). Descriptive names are associated with all keys involved. A CRT display line reports on command activity, while additional feedback is provided by audible beeps at execution, and by other data displays showing the current instrument status.

A choice of five displays are available by operator selection depending on the data required. A full downlink display of all 120 words is available in a decimal format, or more detailed displays of data subsets may be chosen,

which use engineering units for faster interpretation. A 1024 second buffer is available to allow for storage and later examination of all data.

A major enhancement of this generation of the GSE equipment is the capability to perform automatic functional tests. After entering setup data for testing via a prompted routine (ie. operator name, location, equipment, environment, ....), repeated tests may be requested by pressing a single "AUTOTEST" button, which will conduct the ~ 10 minute functional test and automatically print out all test setup, test measurements, and a summary of results. An auxiliary test mode, called critical parameter monitoring, allows the GSE to operate the SSIES-2 for long unattended periods, periodically storing data in a buffer. Special alarming and automatic shutdown is included to prevent damage to the flight equipment.

### **6.3.2 Electronics Rack**

The electronics rack consists of a set of standard OEM data acquisition modules, power supply and custom electronics, combined within a single enclosure. The rack system includes standard modules as well as a set of empty modules to contain the power supply and OLS interface custom elements.

#### **6.3.2.1 Data Acquisition System**

The rack system chosen is manufactured by Acrosystems Inc., and includes their 901 power module, a 992 system control module, a 911 Analog /Digital I/O module and two 915 switch modules. A matching set of blank modules was purchased to contain the power supply and OLS interface custom elements. Communications between the ACRO modules and the computer system are managed by the 992 system control module via a standard IEEE-488 bus. This module contains an Intel 8088 microprocessor employing a proprietary command language. Simple commands sent from the HP computer are interpreted by this module, which in turn, operates the necessary I/O modules and switches, acquires and formats data, and returns data and status messages. A realtime clock-calendar function is also handled by the ACRO unit.

The ACRO 911 I/O module contains four ground-isolated 12 bit A/D converters, and four ground-isolated 12 bit D/A converters. These are general purpose units, and are ideally suited making the widely separated voltage and current measurements required for an SSIES-2. Two ACRO 915 switch modules are used as multiplexers to allow access to all measurement

points. All interface signals (power, digital data, and analog data) are made available to the GSE computer for evaluation.

#### 6.3.2.2 Power Supply/OLS Interface Board

Analytyx designed and produced the custom electronics for the OLS interface board, as well as a rear housing extension, containing a crossover board interconnect between the Acro modules and the SSIES-2 MEP flight unit connectors.

The OLS interface board (AES#2635) was produced to simulate the OLS functions onboard the spacecraft. The following functions include:

- 1) Generate timing and control signals for SSIES-2 MEP
- 2) Generate serial uplink communication
- 3) Receive serial downlink communication
- 4) receive EST signals from the MEP

Communications between the host computer and the OLS board is done via an HP General Purpose Input Output (GPIO) bus, which is a 16 bit parallel I/O bus. Communications between the OLS and the MEP are divided into three categories, including generation of timing information, generation of serial uplink command messages and receiving formatted downlink data.

Many standard OLS signal types are created on this board. The OLS board generates a system clock (SSIESREF), which is a continuous 10kHz clock stream. Once per second, a gated subset clock (SSIESBCK) is employed to transfer downlink data to the OLS as SSIESDAT. SSIESRED is an envelope signal, with the same length as the SSIESBCK clock train, that is the primary 1 second timing tick. It generates an interrupt signal to the system computer, which allows for synchronization of all GSE functions. Command data (SSIESSER) is sent to an MEP via a serial 8 bit data word within an envelope (SSIESENB). Multiple words may be configured as a block for program uploads, and are automatically metered out to an MEP by the GSE command function. The OLS board also monitors the status of the EST analog and digital lines.

The OLS board is mounted on top of a Lambda model LJS-13 28 volt power supply used to power the SSIES-2 MEP. The OLS board is powered using an Acro 981 breadboard module, which contains a +5 volt power

supply. The 2635 assembly is mounted within four Acro blank modules and is integrated with the other Acro modules.

#### 6.3.2.3 Crossover Board

Since the 911 I/O module contains only four D-A converters and four A-D converters, the signals that need to be generated and acquired must share these resources, and need to be switched through the 915 switch modules. The crossover board is used as an interface between the 915 switch module, the 911 I/O module and flight unit connectors J1 - J6 of the SSIES-2 MEP. The crossover board also contains the circuitry used to simulate the DSM loads, when no DSM is available, and the circuitry to turn on the 28 volt supply used to power the MEP.

Figure 6-1 GSE Configuration Diagram

